



Ph. D. DISSERTATION

A Study on the Performance Enhancement of the Cascode FET Mixer Using New Common-Source and -Drain Configuration

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Under the Supervision of Prof. Young Yun

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Department of Radio Communication Engineering Graduate School of Korea Maritime University

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Nomenclature

Φ	:	Electronic flux
θ	:	Phase shift
π	:	Ratio of circumference, Pi, 3.1415926535
ω	:	Angular frequency
As	:	Arsenic, Atomic number 33
В	:	Bandwidth
В	:	Susceptance
dB	:	Logarithmic unit of decibel
dBm	:	Power ratio in decibels of referenced to 1 milliwatt
Ga	:	Gallium, Atomic number 31
G_a	:	Available gain
G_c	:	Conversion gain 945
G_p	:	Power gain 9 CH
G_t	:	Transducer gain
Ι	:	Current
Im.	:	Image part
In	:	Indium, Atomic number 49
Κ	:	Kelvin, Absolute thermodynamic temperature
Р	:	Phosphorus, Atomic number 15
P_{av}	:	Maximum available power
Q	:	Charge of electronic

Re.	:	Real part
Si	:	Silicon, Atomic number 14
S_{ij}	:	Scattering parameter, S-parameter
T_0	:	Standard noise temperature, 290 K
V	:	Voltage
Х	:	Reactance
Y	:	Admittance
Ζ	:	Impedance
Z_L , Z_{out}	:	Load impedance, Output impedance
Z _S , Z _{in}	:	Source impedance, Input impedance
g_m	:	Transconductance
j	:	Imaginary number 45
f	:	Frequency of of the
k	:	Boltzmann's constant, 1.38×10 ⁻²³ J/K

Abbreviation

AM	:	Amplitude Modulation
BJT	:	Bipolar-Junction Transistor
DSB	:	Double Side Band
FET	:	Field-Effect Transistor
HBT	:	Heterojunction Bipolar Transistor
IF	:	Intermediate Frequency
IIP ₃	:	Input 3rd-order Intercept Point
IM	:	Inter-Modulation
IMD	:	Inter-Modulation Distortion
IMR	:	Inter-Modulation Ratio
IP ₃	:	3rd-order Intercept Point
LDMOS	:	Laterally diffused MOSFET
LNA	:	Low Noise Amplifier
LO	:	Local Oscillator
LSB	:	Low-Side Band
MDS	:	Minimum Discernible Signal
MESFET	:	MEtal Semiconductor Field Effect Transistor
MMIC	:	Monolithic Microwave Integrated Circuit
MOSFET	:	Metal Oxide-Semiconductor Field-Effect Transistor
NF	:	Noise Figure
OIP ₃	:	Output 3rd-order Intercept Point

P _{1dB}	:	1-dB Gain Compression Point
рНЕМТ	:	pseudomorphic High Electron Mobility Transistor
РМ	:	Phase Modulation
RF	:	Radio Frequency
RFIC	:	Radio Frequency Integrated Circuit
SSB	:	Single Side Band
USB	:	Up-Side Band

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Abstract

A Study on the Performance Enhancement of the Cascode FET Mixer Using New Common-Source and -Drain Configuration

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The wireless communication system has become highly developed of late due to the emergence of various communication technologies, and it is becoming more widely used due to the various information requirements of its users. It has the advantages of mobility and accessibility due to easy information acquisition anytime and anywhere. Thus, the characteristics of low power consumption and high performance are required for the effective power management of the wireless communication system. It depends on a battery for system operation, however, whose efficiency and capacity for highly effective power management is still being investigated. Therefore, as the wireless communication system has limited power, it certainly requires effective RF circuits with low power consumption.

The goal of this study is to develop a wireless communication system circuit with enhanced RF performance: the cascode FET mixer with new common-source and -drain circuit configuration.

For the high performance of a wireless communication system with low power consumption, a well-designed RF circuit is certainly needed due to its large influence on the performance of the whole wireless communication system. If the mixer circuit is well designed, the whole wireless communication system will exhibit high performance.

In this thesis, the enhanced-performance cascode FET mixer using new common-source and -drain circuit configuration is proposed. When the cascode FET mixer using new configuration was compared with the conventional one, it was found that the former has the performance of higher conversion gain at a lower input LO power, a very low noise figure, and very high LO-to-IF isolation. Thus, the proposed cascode FET mixer with enhanced RF performance can improve the performance of the wireless communication system, which can realize effective power consumption because of the use of a local oscillator with lower output power.

The cascode FET mixer using new configuration was designed in this study based on the results of the simulation and measurement for the verification of the enhanced RF performance. The results showed the mixer's enhanced RF performance compared with the conventional cascode FET mixer. The proposed new common-source and -drain circuit configuration in the cascode FET mixer is reported in this thesis for the first time.

The cascode FET mixer using new configuration showed effective operation by means of the use of a local oscillator with lower output LO power. It also showed higher conversion gain with only the lower input LO power, which does not need a local oscillator with a large output power as it can be operated at lower input LO power compared with the conventional one. This is the important characteristic for the wireless communication system, which requires effective power consumption. The cascode FET mixer using new configuration showed very high LO-to-IF isolation without a LO rejection filter compared with the conventional one. It showed good LO-to-RF isolation. The cascode FET mixer using new configuration also showed a very low noise figure compared with the conventional one. It uses only a FET, which produces the effect to have very low noise figure due to the thermal and shot noise by an active device. The cascode FET mixer using new configuration showed low output IF power and low linearity for the output IF power of the fundamental and third-order intermodulation frequencies, low than those of the conventional one. It also showed the low output IF power spectrum for the intermodulation distortion of the low-side and up-side bands, as opposed to the conventional one. It showed that each reflection coefficients were about -30 dB for the RF frequency of 2.6 GHz, the LO frequency of 2.5 GHz, and the IF frequency of 100 MHz.

Through the aforementioned study results, it is exhibited in this thesis that the proposed cascode FET mixer has enhanced RF performance by means of the new common-source and -drain circuit configuration. It can thus achieve high RF performance without an addition to any other circuit, for the enhancement of the RF performance. Especially, the cascode FET mixer using new configuration showed an indispensable circuit, which it must have to improve the efficiency of the wireless communication system due to the mobility and limited power.

초 록

새로운 공통-소스와 공통-드레인 구조를 이용한 캐스코드 FET 믹서의 성능 향상에 관한 연구

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무선 통신 시스템은 다양한 통신 기술들에 의해서 최근에 매우 발전 되고 있으며, 사용자들의 다양한 정보 요구에 때문에 더 광범위하게 사용 되어지고 있다. 무선 통신 시스템은 언제 어디서나 쉽게 정보를 획득하기 때문에 이동성과 접근성의 장점을 가지고 있다. 따라서 낮은 전력 소비와 높은 성능의 특성들은 무선통신 시스템의 효율적인 전력 관리를 위해서 요구되고 있으며, 이런 특성들은 시스템 동작을 위해서 전원 장치에 의존 하지만, 매우 효과적인 전원 관리를 위한 전원 장치의 효율성과 용량성은 아직도 계속 연구되고 있는 중이다. 그러므로 무선 통신 시스템이 제한된 전원을 가지는 것과 같이 낮은 전력 소비를 가지는 효율적인 무선 주파수 회로들이 반드시 요구된다.

이 연구의 목표는 새로운 공통-소스와 공통-드레인 회로 구조를 가지 는 캐스코드 FET 믹서의 향상된 RF 성능을 가지는 무선 통신 시스템 회 로를 개발하는 것이다. 낮은 전력 소비를 가지는 무선통신 시스템의 높은 성능을 위해서, 잘 설계된 RF 회로는 전체 무선 통신 시스템의 성능에 큰 영향을 미치기 때 문에 반드시 필요하다. 믹서 회로가 잘 설계되었다면, 전체 무선 통신 시 스템은 높은 성능을 보여줄 것이다.

이 논문에서는 새로운 공통-소스와 공통-드레인 회로 구조를 이용해 향상된 성능의 캐스코드 FET 믹서를 제안한다. 새로운 구조를 이용한 캐 스코드 FET 믹서는 기존의 캐스코드 FET 믹서와 비교해서 더 낮은 입력 LO 전력에서 더 높은 변환 이득, 매우 낮은 잡음 지수와 더 높은 LO와 IF간의 격리 특성을 가지는 것이 확인되었다. 이렇게 향상된 RF 성능을 가지는 새로운 구조를 이요한 캐스코드 FET 믹서는 더 낮은 출력 전력을 가지는 국부 발진기의 사용하기 때문에 효율적인 전력 소비를 실현할 수 가 있어서 무선 통신 시스템의 성능을 개선할 수가 있다.

새로운 구조를 이용한 캐스코드 FET 믹서는 향상된 RF 성능의 검증 을 위해서 모의실험과 측정의 결과들에 기반하여 이 연구가 설계되어졌으 며, 이런 결과들은 기존의 캐스코드 FET 믹서와 비교해서 제안된 믹서의 향상된 RF 성능을 보여주었다. 그리고 연구에서 제안하는 새로운 공통-소 스와 공통-드레인 회로 구조를 가지는 캐스코드 FET 믹서는 처음으로 이 논문에서 발표되어지는 것이다.

새로운 구조를 이용한 캐스코드 FET 믹서는 더 낮은 출력 LO 전력을 가지는 국부 발진기의 사용에 의하여 효과적인 동작을 보여주었다. 또한, 제안된 믹서는 기존의 캐스코드 FET 믹서와 비교해서 더 낮은 입력 LO 전력에서 동작할 수 있기에 큰 출력 전력을 가지는 국부 발진기가 필요하 지 않으므로 더 낮은 LO 전력만 가지고도 더 높은 변환 이득을 보여주었 다. 이것은 효과적인 전력 소비를 요구하는 무선 통신 시스템을 위해서 중 요한 특성이다. 새로운 구조를 이용한 캐스코드 FET 믹서는 기존의 캐스 코드 FET 믹서와 비교해서 LO 제거 필터 없이도 매우 높은 LO와 IF간의 격리 특성과 좋은 LO와 RF간의 격리 특성을 보여주었다. 새로운 구조를 이용한 캐스코드 FET 믹서는 또한 기존의 캐스코드 FET 믹서와 비교해서 매우 낮은 잡음 지수를 보여주었으며, 제안된 믹서는 하나의 능동 소자에 의한 열 잡음과 산탄 잡음 때문에 매우 낮은 잡음 지수의 효과를 만드는 하나의 FET만으로 이용한 것이다. 새로운 구조를 이용한 캐스코드 FET 믹 서는 낮은 출력 IF 전력과 기본 주파수와 3차 혼변조 주파수의 출력 IF 전 력을 대해서 낮은 선형성을 보여주었고, 기존의 캐스코드 FET 믹서의 성 능보다 낮게 나타났다. 새로운 구조를 이용한 캐스코드 FET 믹서는 또한 하측파 대역과 상측파 대역의 혼변조 왜곡에 대해서 낮은 출력 IF 전력 스펙트럼을 보여주었으며, 기존의 캐스코드 FET 믹서에 대립되어지는 것 으로 보여주었다. 새로운 구조를 이용한 캐스코드 FET 믹서는 기존의 믹 서와 비교해서 2.6 GHz의 RF 주파수, 2.5 GHz의 LO 주파수와 100 MHz 의 IF 주파수에 대해서 -20 dB보다 낮은 반사 계수 특성을 보여주었다.

앞에서 보여준 연구 결과들을 통하여, 제안된 캐스코드 FET 믹서가 새로운 공통-소스와 공통-드레인 회로 구조의 사용에 의하여 향상된 RF 성능을 가지는 것을 이 연구에서 제시되었다. 이와 같이 새로운 구조를 이 용한 캐스코드 FET 믹서는 RF 성능의 향상을 위해 어떤 다른 회로의 추 가 없이도 높은 RF 성능을 달성할 수가 있다. 특히, 새로운 공통-소스와 공통-드레인 구조를 이용한 캐스코드 FET 믹서는 이동성과 제한된 전원 때문에 무선 통신 시스템의 효율성을 개선하는데 반드시 필요로 한 것이 며, 또한 없어서는 안 되는 회로라는 것을 보여주었다.

Chapter 1.

Introduction



1.1 Background

The wireless communication system has become highly developed of late due to the emergence of various communication technologies, and it is becoming more widely used owing to the various information requirements of its users. It has the advantages of mobility and accessibility due to easy information acquisition anytime and anywhere. An efficient wireless communication system requires low power consumption and high performance, but it is dependent on a battery for its power, whose efficiency and capacity for highly effective power management is still being investigated. Therefore, as the wireless communication system has limited power, it certainly requires highly effective radio frequency (RF) circuits with low power consumption.

The many circuits of a wireless communication system are integrated on one chip, which is called *monolithic microwave integrated circuit* (MMIC) or *radio frequency integrated circuit* (RFIC). For example, MMIC and RFIC are composed of an antenna with the function of selecting the desired frequency signal, a low-noise amplifier (LNA) for decreasing the noise in the received signal and for amplifying only the desired signal, a mixer for converting the frequency based on the signal of the LNA output and that of the local oscillator, and a gain amplifier for amplifying the converted intermediate-frequency (IF) signal.

As shown above, a wireless communication system with RF circuits of low power consumption has higher efficiency compared to the conventional wireless communication system with high power consumption. Especially, the performance of the mixer circuit in a wireless communication system, the transceiver that is used for frequency mixing, differs according to the circuit design, due to its more complicated operation compared to other circuits. It is a significant circuit as it heavily influences the whole wireless communication system. Also, the mixer circuit for frequency mixing needs an LO circuit with higher power consumption compared to other circuits. Thus, if the LO circuit has low power consumption, the power consumption efficiency of the wireless communication system increases

As for the features of other mixer circuits, the resistive mixer circuit has the advantage of lower power consumption compared to the active mixer, but it needs an additional gain amplifier because it has very low conversion loss, lower than that of the active mixer. The resistive mixer with an additional gain amplifier has high power consumption because of its many active devices [1-4].

Therefore, the mixer circuit requires circuit development for the enhanced performance and low power consumption of the wireless communication system. For the design of the high-performance mixer and of the active device fabricated through the semiconductor fabrication process, it was decided that a field effect transistor (FET) and a bipolar-junction transistor (BJT) be fabricated on the semiconductor substrate through the fabrication process of gallium arsenide (GaAs) and silicon (Si). The mixer of high performance was achieved by the most active device, but the commercial products showed no performance difference due to the recently developed advanced semiconductor process technology. The selection of the transistor is important for the design of a high-performance mixer because the metal semiconductor field effect transistor (MESFET) and pseudomorphic high electron mobility transistor (pHEMT) of FET devices are voltage-controlled devices with a high-speed switching property, and the heterojunction bipolar transistor (HBT) of BJT devices is a current-controlled device with a high current transfer property. The FET devices are used by most mixer circuits due to their high-speed switching property, higher than that of the BJT devices. Thus, it is a widely used circuit for higher-frequency operation.

For a high-performance RF circuit, a well-designed circuit is certainly needed because it heavily influences the performance of the wireless communication system. Especially, if the mixer circuit is well designed, the whole wireless communication system is expected to exhibit high performance and power efficiency [5-8].

The goal of this study is to propose an enhanced-performance cascode FET mixer that uses a new common-source and -drain circuit configuration for the enhanced RF performance of a wireless communication system. It has higher conversion gain, a very low noise figure, and very high LO-to-IF isolation without the use of an LO rejection filter for LO signal leakage compared with the conventional mixer. The cascode FET mixer using new configuration has higher conversion gain with only a lower LO power, as opposed to the conventional mixer, which needs high power. There is no need to have a local oscillator circuit with high power consumption; it is possible to realize high power efficiency of the whole wireless communication system because of the use of a local oscillator circuit with low power consumption. The cascode FET mixer using new configuration also has a very low noise figure compared with the conventional mixer because of the thermal and shot noise by only a FET, as opposed to the conventional mixer, which has a high noise figure because of the thermal and shot noise by two FET. The cascode FET mixer using new configuration has very high LO-to-IF isolation compared with the conventional mixer, without the use of a LO rejection filter. The conventional mixer, however, certainly needs a LO rejection filter due to the leakage of the LO signal with very high power at the IF port.

As for the disadvantages of the cascode FET mixer that uses a new common-source and -drain circuit configuration, the cascode FET mixer using new configuration has low linearity because it uses only the g_m of FET 1, as opposed to the conventional mixer, which uses the g_m of FET 1 and 2. The conventional mixer is known to have high linearity, which is a good RF frequency response due to the common-source and -gate configuration. The cascode FET mixer using new

configuration, however, has the advantages of higher conversion gain, a very low noise figure, and very high LO-to-IF isolation without an LO rejection filter, as opposed to the conventional mixer.

In this thesis, an enhanced-performance cascode FET mixer was fabricated using a new common-source and -drain circuit configuration, due to its various advantages compared with the conventional mixer. It showed enhanced RF performance under the same conditions by means of circuit design. It is an indispensable circuit for the wireless communication system, which requires low power consumption for high RF performance in the low-power LO signal compared with the conventional one. Further, it can improve the whole performance of the wireless communication system, and can realize effective power consumption.



1.2 Method of study

In this study, the RF performance of the cascode FET mixer that uses a new common-source and -drain circuit configuration was verified and compared with that of the conventional cascode FET mixer, which uses a common-source and -gate circuit configuration.

The RF characteristics were estimated by design, simulation, and measurement under the same conditions, which were the use of an active device using pHEMT and the DC bias condition for V_{dd} and V_{gs} .

The following were observed in the proposed mixer: the RF performance, conversion gain by an LO signal with power variation, LO-to-RF isolation by an LO signal with power variation, LO-to-IF isolation due to an LO signal with power variation, the P_{1dB} of the RF signal with power variation, the input third-order intercept point (IIP₃), the output third-order intercept point (OIP₃) of an RF signal with power variation and with two-tone frequency, the noise figure of an LO signal with power variation, and the reflection coefficient of each port by the overall operation frequency, for the verification of the performance of the proposed mixer.

The study method included investigation and comparison of the RF characteristics of the proposed cascode FET mixer and the conventional mixer. Accordingly, the proposed cascode FET mixer that uses a new common-source and -drain circuit configuration is expected to exhibit higher RF performance compared to the conventional one.

Chapter 2.

Fundamental Concepts and Definition

of Mixer



2.1. Definition of linearity and nonlinearity

All electronic circuits are nonlinear, which is a fundamental truth of electronic engineering. The linear assumption that underlies most modern circuit theory is in practice only an approximation. Some circuits, such as small-signal amplifiers, are only very weakly nonlinear, however, and are used in systems as if they were linear. In these circuits, nonlinearities are responsible for phenomena that degrade system performance and must be minimized. Other circuits, such as frequency multipliers, exploit the nonlinearities in their circuit elements; these circuits would not be possible if nonlinearities did not exist. In these, it is often desirable to maximize the effect of the nonlinearities, and even to minimize the effects of annoying linear phenomena. The problem of analyzing and designing such circuits is usually more complicated than for linear circuits.

The nonlinearities of solid-state devices are well known, but it is not generally recognized that even passive components such as resistors, capacitors, and inductors, which are expected to be linear under virtually all conditions, are nonlinear in the extremes of their operating ranges. When large voltages or currents are applied to resistors, for example, heating changes their resistances. Capacitors, especially those made of semiconductor materials, exhibit nonlinearity, and the nonlinearity of iron- or ferrite-core inductors and transformers is legendary. Even RF connectors have been found to generate intermodulation distortion at high power levels; the distortion is caused by the nonlinear resistance of the contacts between dissimilar metals in their construction. Thus, the linear circuit concept is an idealization, and a full understanding of electronic circuits, interference, and other aspects of electromagnetic compatibility requires an understanding of nonlinearities and their effects.

Linear circuits are defined as those for which the superposition principle holds.

Specifically, if excitations x_1 and x_2 are applied separately to a circuit having responses y_1 and y_2 , respectively, the response to the excitation $ax_1 + bx_2$ is $ay_1 + by_2$, where a and b are arbitrary constants, which may be real or complex, time-invariant or time-varying. This criterion can be applied to either circuits or systems. This definition implies that the response of a linear, time-invariant circuit or system includes only those frequencies present in the excitation waveforms. Thus, linear, time-invariant circuits do not generate new frequencies. (Time-varying circuits generate the mixing products between the excitation frequencies and the frequency components of the time waveform.) As nonlinear circuits usually generate a remarkably large number of new frequency components, this criterion provides an important dividing line between linear and nonlinear circuits.

Nonlinear circuits are often characterized as either strongly nonlinear or weakly nonlinear. Although these terms have no precise definitions, a good working distinction is that a weakly nonlinear circuit can be described with adequate accuracy by a Taylor series expansion of its nonlinear current/voltage (I/V), charge/voltage (Q/V), or flux/current (Φ/I) characteristic around some bias current or voltage. This definition implies that the characteristic is continuous, has continuous derivatives, and, for most practical purposes, does not require more than a few terms in its Taylor series. (The excitation level, which affects the number of terms required, also must not be too high.) Additionally, we usually assume that the nonlinearities and RF drive are weak enough that the DC operating point is not perturbed. Virtually all transistors and passive components satisfy this definition if the excitation voltages are well within the component's normal operating ranges; that is, well below saturation. Examples of components that do not satisfy this definition are strongly driven transistors and Schottky-barrier diodes, because of their exponential I/V characteristics; digital logic gates, which have input/output transfer characteristics that vary abruptly with input voltage, and step-recovery diodes, which have very strongly nonlinear capacitance/voltage characteristics under forward bias. If a circuit is weakly nonlinear, relatively straightforward techniques, such as power-series or Volterra-series analysis, can be used. Strongly nonlinear circuits are those that do not fit the definition of weak nonlinearity; they must be analyzed by harmonic balance or time-domain methods. These circuits are not too difficult to handle if they include only single-frequency excitation or comprise only lumped elements. The most difficult case to analyze is a strongly nonlinear circuit that includes a mix of lumped and distributed components, arbitrary impedances, and multiple excitations.

Another useful concept is *quasilinearity*. A quasilinear circuit is one that can be treated for most purposes as a linear circuit, although it may include weak nonlinearities. The nonlinearities are weak enough that their effect on the linear part of the circuit's response is negligible. This does not mean that the nonlinearities themselves are negligible; they may still cause other kinds of trouble. A small-signal transistor amplifier is an example of a quasilinear circuit, as is a varactor-tuned filter.

Two final concepts we will employ from time to time are those of *two-terminal nonlinearities* and *transfer nonlinearities*. A two-terminal nonlin- earity is a simple nonlinear resistor, capacitor, or inductor; its value is a function of one independent variable, the voltage or current at its terminals, called a *control voltage* or *control current*. A transfer nonlinearity is a nonlinear controlled source; the control voltage or current is somewhere in the circuit other than at the elements terminals. It is possible for a circuit element to have more than one control, one of which is usually the terminal voltage or current. Thus, many nonlinear element's must be treated as combinations of transfer and two-terminal nonlinearities. An example of a transfer nonlinearity is the nonlinear controlled current source in the equivalent

circuit of a FET, where the drain current is a function of the gate voltage. Real circuits and circuit elements often include both types of nonlinearities. In example, the complete FET equivalent circuit included nonlinear capacitors with multiple control voltages, transconductance, and drain-to-source resistance.



Figure 2.1 (a) Two-terminal nonlinearity, (b) Transfer nonlinearity.

The need to distinguish between the two types of nonlinearities can be illustrated by an example. Figure 2.1 (a) is considered a nonlinear resistor, and Fig. 2.1 (b) is a nonlinear but otherwise ideal transconductance amplifier. Both are excited by a voltage source having some internal impedance R_s . The amplifier's output current is a function of the excitation voltage and the nonlinear transfer function; the current can be found simply by substituting the voltage waveform into the transfer function. In the two-terminal nonlinearity, however, the excitation voltage generates current components in the nonlinear resistor at new frequencies. These components circulate in the rest of the circuit, generating voltages at those

new frequencies across R_s and therefore across the nonlinear resistor. These new voltage components generate new current components, and current and voltage components at all possible frequencies are generated.



2.2. Definition of frequency generation

The traditional way of showing how new frequencies are generated in nonlinear circuits is to describe the component's I/V characteristic by a power series, and to assume that the excitation voltage has multiple frequency components.

Figure 2.2 shows a circuit with excitation V_s and a resulting current *I*. The circuit consists of a two-terminal nonlinearity, but because there is no source impedance, $V = V_s$, and the current can be found by substituting the source voltage waveform into the power series.



Figure 2.2 Two-terminal nonlinear resistor excited directly by a voltage source. Mathematically, the situation is the same as that of the transfer nonlinearity of Fig. 2.1 (b). The current is given by the expression

where a, b, and c are constant, real coefficients. We assume that V_s is a two-tone excitation of the form

Substituting (2.1) into (2.2) gives, for the first term,

(2.3)

 $(\mathbf{0}, \mathbf{1})$

After doing the same with the second term, the quadratic, and applying the well-known trigonometric identities for squares and products of cosines, we obtain

(2.4)

and the third term, the cubic, gives

(2.5)

The total current in the nonlinear element is the sum of the current components in (2.3) through (2.5). This is the short-circuit current in the element; it consists of a remarkable number of new frequency components, each successive term in (2.1) generating more new frequencies than the previous one; if a fourth- or fifth-order nonlinearity were included, the number of new frequencies in the current would be even greater. However, in this case, there are only two frequency components of voltage, at ω_1 and ω_2 , because the voltage source is in parallel with the nonlinearity. If there were a resistor between the voltage source and the nonlinearity, even more voltage components would be generated via the currents in that resistor, those new voltage components would be, theoretically, infinite. In order to have a tractable analysis, it then would be necessary to ignore all frequency components beyond some point; the number of components retained would depend upon the strength of the nonlinearity, the magnitude of the excitation

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voltage, and the desired accuracy of the result.

The generated frequencies shows that all occur at a linear combination of the two excitation frequencies; that is, at the frequencies

where m, n = ..., -3, -2, -1, 0, 1, 2, 3, ... The term $\omega_{m,n}$ is called a *mixing frequency*, and the current component at that frequency (or voltage component, if there were one) is called a *mixing product*. The sum of the absolute values of m and n is called the *order of the mixing product*. For the m, n to be distinct, ω_1 and ω_2 must be *noncommensurate*; that is, they are not both harmonics of some single fundamental frequency. We will usually assume that the frequencies are noncommensurate when two or more arbitrary excitation frequencies exist.

An examination of (2.3) through (2.5) shows that a *k*th-degree term in the power series (2.1) produces new mixing frequencies of order *k* or below; those mixing frequencies are *k*th-order combinations of the frequencies of the voltage components at the element's terminals. This does not, however, mean that m + n < k in every nonlinear circuit. In the above example, the terminal voltage components were the excitation voltages, so only two frequencies existed. However, if the circuit of Fig. 2.1 included a resistor in series with the nonlinear element, the total terminal voltage would have included not only the excitation frequencies, but higher-order mixing products as well. The nonlinear element then would have generated all possible *k*th-order combinations of those mixing products and the excitation frequencies. Thus, in general, a nonlinear element can generate mixing frequencies involving all possible harmonics of the excitation frequencies, even those where m + n is greater than the highest power in the power series. It does this by generating *k*th-order mixing products between all the frequency components of its terminal voltage.
Another conclusion one may draw from (2.3) through (2.5) is that the odd-degree terms in the power series generate only odd-order mixing products, and the even-degree terms generate even-order products. This property can be exploited by balanced structures. Balanced circuits combine nonlinear elements in such a way that either the even- or odd-degree terms in their power series are eliminated, so only even- or odd-order mixing frequencies are generated. These circuits are very useful in rejecting unwanted even- or odd-order mixing frequencies.

The generation of apparently low-order mixing products from the high-degree terms in (2.1) is worth some examination, the terms at ω_1 and ω_2 in (2.5) exemplify this phenomenon. The existence of these terms implies that the fundamental current, for example, is not solely a function of the excitation voltage and the linear term in (2.1), it is dependent on all the odd-degree nonlinearities. Consequently, as V_s is increased, the cubic term becomes progressively more significant, and the fundamental-frequency current components either rise more rapidly or level off, depending on the sign of the coefficient *c*. A closer inspection of these terms shows that they can be considered to have arisen from the *k*th-degree term as *k*th-order mixing products; for example, the ω_1 terms in (2.5) arise as the third-order combinations

(2.7)

The presence of the negative frequencies might be more convincing if the cosine functions were expressed in their exponential form, $cos(\omega t) = (exp(j\omega t) + exp(-j\omega t))/2$. Thus, when dealing with nonlinear circuits, one must always use a system of analysis that does not exclude the presence of negative frequencies.

In summary, the I/V characteristic of a nonlinear circuit or circuit element often can be characterized by a power series. The *k*th-degree term in the series generates *k*th-order mixing products of the frequencies in its control voltage or current. Some of these may coincide with lower-order frequencies. Mixing products may also coincide with higher-order frequencies; these are generated as *k*th-order mixing products between other mixing products. Thus, in general a nonlinear circuit having both even- and odd-degree nonlinearities in its power series generates all possible mixing frequencies, regardless of the maximum degree of its nonlinearities.

A special case of the nonlinear circuit having two-tone excitation occurs where one tone is relatively large, and the other is vanishingly small. This situation is encountered in microwave mixers, where the large tone is the LO, and the small one is the RF excitation. Because the RF excitation is very small, its harmonics are negligibly small, and we can assume that only its fundamental-frequency component exists. The resulting frequencies are

which can also be expressed by our preferred notation,

(2.9)

where n = ..., -3, -2, -1, 0, 1, 2, 3, ... and $\omega_0 = |\omega_{RF} - \omega_{LO}|$ is the mixing frequency closest to DC; in a mixer, ω_0 is often the IF, the output frequency. In (2.8) and (2.9) the mixing frequencies are above and below each LO harmonic, separated by ω_0 .

If the total small-signal voltage v(t) is much smaller than the LO voltage $V_L(t)$, the circuit can be assumed to be linear in the RF voltage. The total large-signal and small-signal current I(t) in the nonlinearity of (2.1) is given by

Separating the small-signal part of (2.10), and assuming that $v^2(t) \ll v(t)$, we find the small-signal current i(t) to be

This is a linear function of v, even though many of the current components in (2.11) are at frequencies other than the RF. Thus, a microwave mixer, which has an input at RF and output at, for example, ω_0 , is a quasilinear component in terms of its input/output characteristics under small-signal excitation.



2.3 Nonlinear phenomena

2.3.1 Harmonic generation

One obvious property of a nonlinear system is its generation of harmonics of the excitation frequency or frequencies. These are evident as the terms in (2.3) through (2.5) at $m\omega_1$, $m\omega_2$. The *m*th harmonic of an excitation frequency is an *m*th-order mixing frequency. In narrow-band systems, harmonics are not a serious problem because they are far removed in frequency from the signals of interest and inevitably are rejected by filters. In others, such as transmitters, harmonics may interfere with other communications systems and must be reduced by filters or other means.

2.3.2 Intermodulation distortion

All the mixing frequencies in (2.3) through (2.5) that arise as linear combinations of two or more tones are often called *intermodulation products*. The IM products generated in an amplifier or communications receiver often present a serious problem, because they represent spurious signals that interfere with, and can be mistaken for, desired signals. The IM products are generally much weaker than the signals that generate them; however, a situation often arises wherein two or more very strong signals, which may be outside the receiver's passband, generate an IM product that is within the receiver's passband and obscures a weak, desired signal. Even-order IM products usually occur at frequencies well above or below the signals that generate them, and consequently are often of little concern.

The IM products of greatest concern are usually the third-order ones that occur at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, because they are the strongest of all odd-order products, are close to the signals that generate them, and often cannot be rejected by filters. Intermodulation is a major concern in microwave systems.

2.3.3 Saturation and desensitization

The excitation-frequency current component in the nonlinear circuit examined in Section 2.2 was a function of power series terms other than the linear one; recall that (2.5) included components at ω_1 and ω_2 that varied as the cube of signal level. Such components are responsible for gain reduction and desensitization in the presence of strong signals.

In order to describe saturation, we refer to (2.1) to (2.5). From (2.3) and (2.5), and with $V_2 = 0$, we find the current component at ω_1 , designated $i_1(t)$, to be

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(2.12)

If the coefficient c of the cubic term is negative, the response current saturates; that is, it does not increase at a rate proportional to the increase in excitation voltage. Saturation occurs in all circuits because the available output power is finite. If a circuit such as an amplifier is excited by a large and a small signal, and the large signal drives the circuit into saturation, gain is decreased for the weak signal as well. Saturation therefore causes a decrease in system sensitivity, called *desensitization*.

2.3.4 Cross modulation

Cross modulation is the transfer of modulation from one signal to another in a nonlinear circuit. To understand cross modulation, imagine that the excitation of the circuit in Fig. 1.1 is

where m(t) is a modulating waveform; |m(t)| < 1. Equation (2.13) describes a

combination of an unmodulated carrier and an amplitude-modulated signal. Substituting (2.13) into (2.1) gives an expression similar to (2.5) for the third-degree term, where the frequency component in $i_c(t)$ at ω_1 is

where a distorted version of the modulation of the ω_2 signal has been transferred to the ω_1 carrier. This transfer occurs simply because the two signals are simultaneously present in the same circuit, and its seriousness depends most strongly upon the magnitude of the coefficient *c* and the strength of the interfering signal ω_2 . Cross modulation is often encountered on an automobile AM radio when one drives past the transmission antennas of a radio station; the modulation of that station momentarily appears to come in on top of every other received signal.

2.3.5 AM-to-PM conversion

AM-to-PM conversion is a phenomenon wherein changes in the amplitude of a signal applied to a nonlinear circuit cause a phase shift. This form of distortion can have serious consequences if it occurs in a system in which the signal's phase is important; for example, phase- or frequency-modulated communication systems. The response current at ω_1 in the nonlinear circuit element is, from (2.3) and (2.5),

where $i_1(t)$ is the sum of first- and third-order current components at ω_1 . Suppose, however, these components were not in phase. This possibility is not predicted by (2.1) through (2.5) because these equations describe a memoryless nonlinearity. In a circuit having reactive nonlinearities, however, it is possible for a phase difference to exist. The response is then the vector sum of two phasors,

where θ is the phase difference. Even if θ remains constant with amplitude, the phase of I_1 changes with variations in V_1 . It is clear from comparing (1.16) to (1.12) that AM-to-PM conversion is most serious as the circuit is driven into saturation.

2.3.6 Spurious responses

In mixer, with an RF input at ω_{RF} and an LO at ω_{LO} , has currents at the frequencies given by (2.8) or (2.9). It is easy to see that, if the RF is applied at any of those mixing frequencies, currents at all the rest are generated as well. Thus the mixer has some response at a large number of frequencies, not just the one at which it is designed to work. In fact, if the applied signal is very strong, its harmonics are generated and the mixer has spurious responses at any frequency that satisfies the relation

where m and n can both be either positive or negative integers. Comparing (2.17) to (2.6) shows that spurious responses are a form of two-tone intermodulation wherein one of the tones is the LO. In microwave technology the concept of spurious responses is used only in reference to mixers.

2.3.7 Adjacent channel interference

In many communications systems, especially those used for cellular telephones and other forms of telecommunications, modulated signals are squeezed into narrow, contiguous channels. Nonlinear distortion can generate energy that falls outside the intended channel. This is called *adjacent-channel interference*, *spectral regrowth*, or sometimes *co-channel interference*.

Adjacent-channel interference is fundamentally odd-order intermodulation distortion, and, like most odd-order IM, it is dominated by third-order effects, although higher-order nonlinearities may also contribute. The phenomenon is easy to understand. The third-order system shows that the output is simply the sum of all possible third-order intermodulation products involving any three-fold combination of excitation frequency components. Like simple third-order intermodulation involving two excitation tones, many of these components fall close to the original excitation spectrum. These components cause adjacent-channel interference. Many components can also fall within the excitation channel as well, distorting the modulated signal.



2.4 Definition of power and gain

Although it is customary to speak loosely of gain and power in microwave circuits, these quantities can be defined in several different ways. The different definitions of gain are related to the concepts of *available* and *dissipated power*.

These concepts are important in both linear and nonlinear circuits, although they are particularly important in nonlinear circuits, where a waveform may have components at many frequencies that may or may not be harmonically related.



Figure 2.3 Circuit having a matched source and load.

Available or transferable power is the maximum power that can be obtained from a source. The concept of available power is illustrated in Fig. 2.3, in which a sinusoidal voltage source having a peak value V_s has an internal impedance of R_1 + jX_1 (unless we state otherwise, all frequency-domain voltages and currents in this Section are phasor quantities; thus, their magnitudes are equal to peak sinusoidal quantities, not RMS).

The maximum power is obtained from this source if the load impedance equals the conjugate of the source impedance, $Z_L = Z_s^* = R_I - jX_I$. Under these conditions,

(2.18)

where I is the peak value of the current, i(t). The power dissipated in the load, P_d , is

which is the maximum available from the source, P_{av} .



Figure 2.4 Circuit having an unmatched source and load.

Dissipated, or transferred power is the power dissipated in a load that may or may not be matched to the source. In Fig. 2.4, the load is not conjugate-matched to the source, so the dissipated power is somewhat less than that given in (2.19). In this case,

and the power dissipated in the load is

In a nonlinear circuit the voltage source may contain many frequency components, and the source or load impedance may not be the same at each frequency. An example of this situation is the output circuit of a diode frequency multiplier. The multiplier generates many harmonics, all but one of which is undesired, so it has an output filter that allows only the desired harmonic to reach the output port. Thus, the impedance presented to the diode at the desired output frequency is the load impedance, but at all other harmonics it is the out-of-band impedance of the filter. The current in the loop is a function of frequency, as shown in Fig. 2.5.



Figure 2.5 Unmatched circuit having a nonsinusoidal voltage-source excitation.

Because the load and source are linear, each frequency component can be treated separately without concern for the others. Then the available and transferred power are

An equivalent representation uses a current source and admittances as shown in Fig. 2.6. Similarly, the available and dissipated powers are found to be





Figure 2.6 Unmatched circuit having a nonsinusoidal current-source excitation.



Figure 2.7 Model of a voltage source and load, where the excitation has a number of discrete frequency components.

Figure 2.7 shows a model often used when a voltage (or current) source has many discrete frequency components. The load impedance at each frequency is represented by an impedance in series with a filter. The filters F_1 , F_2 , ..., F_N are ideal series-resonant circuits; that is, they are short circuits at their resonant frequencies and open circuits at all other frequencies. Thus, the current component at only one frequency circulates in each branch. One of these branches is the output circuit; the rest may be arbitrary impedances that represent the combined effects of out-of-band filter or matching circuit terminations, package or other circuit parasitics, or in some cases resonances (called *idlers*) that are purposely introduced to optimize performance. The terminations at intermediate frequencies may have a strong effect upon the circuit's performance, so the design of the output network may have to account for those terminations as well as the one at the output frequency.

The gain of a two-port network can be defined in terms of available and dissipated powers. The two most important gain definitions are *transducer gain* and *maximum available gain*. This is precisely the definition of *transducer gain*. Thus,

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(2.26)

where G_t is the transducer gain.

Transducer gain is a very useful concept because, in microwave systems, it is most important to know how much more or less power a circuit delivers to a standard load (e.g., a 50 Ω coaxial termination), compared to the power that could have been obtained from the source alone. This is precisely what transducer gain tells us. Furthermore, transducer gain is almost always a defined quantity, because it requires only that the source and output powers be finite, and real sources always have finite available power. Thus, the concept is handy in nonlinear circuits where, as our earlier discussion of large-signal S parameters illustrated, it is often impossible to define input and output impedances or reflection coefficients.

Other gain definitions are often useless because they do not tell the engineer what he wants to know, or occasionally result in meaningless or undefined quantities. One such concept is *power gain*, G_p , defined as power delivered to the load divided by power delivered to the two-port's input; thus,

We find that the power gain of a low-frequency MESFET amplifier, for example, is meaninglessly high: the FET's output power is modest, but its input impedance is highly reactive, so the input power is close to zero. This result tells nothing about the way the amplifier works in a system. The concept of power gain can give even more bizarre results when applied to other circuits, such as a negative-resistance amplifier without a circulator. The input power of a negative-resistance device is difficult to define, but one could justifiably say that it is negative and equal to the output power. Thus, the power gain of a negative-resistance amplifier is always -1. Even with these strange results, however, the concept of power gain has some limited usefulness; one of these uses the design of linear amplifiers that have prescribed values of transducer gain.

Available gain, G_a , is defined as the power available from the output divided by the power available from the source; thus,

Available gain is intrinsically not a very useful concept (although it will costar with power gain), but its maximum value, called the *maximum available gain*, which occurs when the input of the two-port is conjugate-matched to the source, is very useful. The maximum available gain is, therefore, the highest possible value of the transducer gain, which occurs when both the input and output ports are conjugate-matched. Maximum available gain is defined only if the two-port is unconditionally stable; that is, if the input and output impedances always have positive real parts when any passive load is connected to the opposite port.

2.5 Stability

The fundamental definition of a stable electrical network is that its response is bounded when the excitation is bounded. In the case of a linear two-port having a sinusoidal steady-state excitation, this definition leads to a stability criterion: the network's poles must all be in the left half of the complex plane. A stable linear network can be made unstable through an unfortunate choice of source or load impedance; much of the "stability theory" of microwave circuits deals with this possibility, rather than the inherent stability of the circuit itself.

The situation is more complicated in the case of nonlinear circuits. Because the kinds of interactions that can occur in nonlinear circuits are more complex than in linear ones, such circuits often exhibit transient and steady-state phenomena other than sinusoidal oscillation, which, although bounded, are loosely classed as instability. These include parasitic oscillations; spurious outputs that occur only under large-signal excitation; "snap" phenomena, in which the output level or bias conditions change abruptly as input level is varied; chaotic behavior; and the exacerbation of normal noise levels. These may depend on initial conditions; some initial conditions may result in a stable response, others not, so it is strictly correct to speak only of a stable *solution*, not a stable *circuit*. Of course, plain, old-fashioned oscillation is also a possibility. Consequently, it is extremely difficult to devise a meaningful and practical stability criterion for nonlinear circuits.

Even without the academic advantage of a stability criterion, it is usually possible, with care, to design nonlinear or quasilinear circuits that are well-behaved. For example, if a harmonic-balance analysis of a proposed circuit design converges without incident to a solution, one can be confident that it is, by all practical definitions of the term, stable. (It is also stable in theory, because harmonic-balance analysis is a process of perturbing the voltages across the nonlinear elements. If these perturbations do not cause larger perturbations, the circuit must be locally stable. The idea that a circuit is stable if such perturbations do not cause greater perturbations is equivalent to the concept of stability defined earlier.) The converse may not be true, however, because the failure of an iterative technique such as harmonic balance to converge may be caused by numerical problems, not by inherent instability.

In oscillators, we have yet another concept of stability. At start-up, an oscillator is an unstable, linear circuit; it must have poles in the right half plane. However, once the oscillation is established, it must be stable, in the sense that it remains in a steady state and returns to that steady state after any small perturbation. This is a loose description of a concept known as *Liapunov stability*.



2.6 Performance concept of mixer

2.6.1 Conversion gain and loss

As shown in Fig. 2.8, a mixer is a three-port device, which in addition to the input RF signal port and output IF signal port, uses a third LO port to drive the mixer. This driving action, sometimes called switching or modulation because of its impact on the mixer device, is highly nonlinear and causes either the device conductance or transconductance to switch between two states, one with a low transconductance and the other with a high transconductance.



Figure 2.8 The frequency generation of mixer model.

The almost all mixers use either a time-variant conductance or a time-variant transconductance nonlinearity to achieve frequency translation. In part, we will use the variable g(t) to represent this time-variant nonlinearity.

The switching between the two states occurs at the local oscillator frequency f_{LO} , so the (trans)conductance waveform will contain at least a fundamental component, and possibly higher harmonics as well. If the local oscillator signal is strong enough to cause the device to become nonlinear, then we may write

where $\omega_{LO} = 2\pi f_{LO}$. For instance, if the device is switched between an on and a perfect off state, the (trans)conductance waveform is square, with minimum value zero and maximum value corresponding to the on-conductance g_{ON} . In that case, (2.29) would become

The mixer is in the baluns or combiners that simultaneously impress the strong LO switching waveform across the mixer added to the much smaller RF input signal, $v_{RF} \cdot cos(\omega_{RF}t)$, where $\omega_{RF} = 2\pi f_{RF}$. The term balun is generally used for the three- or four-port device that is configured to linearly sum the incident voltages at the two balun input ports (the LO and RF), rather than for achieving single-ended to differential conversion as is commonly the case in other types of circuits. Of course, the same circuit can often be used for either function.

The effective voltage applied across the time-varying conductance is then the input signal voltage. For although the mixer model in Fig. 2.8 shows three ports, diodes have only two terminals and transistors three, so some means of feeding the device with two signals and for extracting the third needs to be created. If this can be done, then the output current of interest is simply

The RF signal has been translated in frequency, and its phase and amplitude are preserved in the Fourier components of the output current waveform. In theory, the LO carrier has been suppressed at the output. However, the expression implies that we must carefully consider the harmonic embedding impedances of the diode in order to preserve the conductance relationship and to select the desired output components. For a down-converter, we are generally interested in the IF component at radian frequency $\omega_{LO} - \omega_{RF}$, the difference between the local oscillator and the RF component. For an upconverter, it is the IF component at frequency $\omega_{LO} + \omega_{RF}$ that is of interest. The amplitude of the desired IF current component is then $(g_I / 2) \cdot v_{RF}$, which is linearly related to the input RF signal strength.

As a rule, we should consider at the very least the IF, RF, and LO matching impedances of the device. Often, the higher harmonic current components will be short-circuited by the parasitic impedances of the device itself, although not always. As long as (2.29) is not corrupted by doing so, short-circuit matching impedances at unwanted frequencies are generally preferred because they will prevent any unwanted distortion voltages that could arise from remixing within the device, and result in better intermodulation performance. In (2.29), the incremental conductance g is defined as $\partial I / \partial V$ or $\partial I_O / \partial V_{IN}$ in the case of transconductance.

Now in the simple case of a square-law device, the total input current to the device *I* is expressed as a second-order power series of the total voltage *V* across it,

so that

(2.33)

If we let $V(t) = V_{LO} \cdot cos(\omega_{LO})t$, then comparing (2.29) and (2.33) gives in this case $g_0 = G_1$ and $g_1 = 2G_2 \cdot V_{LO}$. Thus, in this simplest case. The desired IF component $(g_1/2) \cdot v_{RF}$ depends on the second-order nonlinearity G_2 in the transfer characteristic of the device. This makes modeling of mixers more difficult than amplifiers, where the fundamental output depends instead principally on G_1 , the linear transconductance term. The desired IF component of current is linearly related to the input signal v_{RF} .

In higher-order devices, differentiation of the equivalent of (2.32) produces terms in $(n+1) \cdot G_{n+1} \cdot V(t)^n$, which upon expansion of the LO voltage term $V_{LO}^n \cdot cos^n(\omega_{LO}t)$ into its harmonic components will produce additional components $V_{LO}^k \cdot cos(k\omega_{LO}t)$, k = 0, 1,... that will change the values of g_0, g_1 , and so on, and introduce additional dependency on the LO signal level. However, the principle of (2.31) still stands, so that sum and difference frequencies will flow in the mixer current and the difference frequency component will still be linearly related to the input RF voltage.

We have overlooked one assumption that is not quite negligible, and that is that the RF voltage itself is part of the total applied voltage in (2.32). Although generally negligible compared to the much larger LO voltage, it will, in fact, be impressed across the device and as a result, g(t) in (2.33), and the coefficients g_0 , g_1 , and so on will also have a weak dependency on the RF signal. This introduces harmonic terms in the RF frequency ω_{RF} in a similar way to ω_{LO} , as well as introduces dependency on the magnitude and phase of the RF voltage, so that the mixer now shows nonlinear dependence on the RF component. Thus, in general, the output current of a mixer will contain terms at frequencies

Provided the LO voltage is much stronger than the RF voltage, the output current term at the difference frequency is linearly related in amplitude and phase to the input RF signal. This frequency, the IF component, has m = n = 1.

As shown in Fig. 2.9, the LO can be either below the RF band of interest, in which case the mixer is referred to as the low-side down-converter, or above it, resulting in the high-side down-converter. The difference between the IF in the high-side down-converter and the IF in the low-side down-converter is that the phase of the two IF signals will be 180° apart. In the second case $\omega_{LO} - \omega_{RF}$ will be positive and in the first case will be negative, since if $\omega_{LO} > \omega_{RF}$, then $sin(\omega_{RF} - \omega_{LO})t = sin[(\omega_{LO} - \omega_{RF})t + \pi]$.

The implications of the "±" term in (2.34) are important. In down-converters, it implies that any undesired RF components at an image frequency of $\omega_{LO} - \omega_{IF}$ (for LO below the desired RF) or $\omega_{LO} + \omega_{IF}$ (for LO above the desired RF) will also be down-converted to the IF.

Figure 2.9 illustrates this case. The down-conversion of an image frequency has implications for both the system noise floor and spurious response.

In up-converters, the " \pm " term implies that the signal is mixed to both a lower and an upper sideband, as shown in Fig. 2.10 for up-conversion of the IF to RF.

Note that an upconverter can be either a sum or a difference mixer, depending on the sideband selected.

Although up-converters are frequently referred to as modulators in a transmitter (as

shown in the Fig. 2.9 and 2.10), up-converters are also useful in receivers where the RF band covers a large percentage bandwidth and down-conversion would require a large percentage tuning range for the VCO, or cause problems with the image frequency lying in band.



Figure 2.9 The mixer of down-converter system.



Figure 2.10 The mixer of up-converter system.

As shown above Fig. 2.10, mixers are characterized by comparing the relation between the output current, generally at the IF frequency, to the input RF voltage. In terms of power, the *conversion gain* is defined for a mixer as simply

For passive mixers, such as diode mixers, there is always conversion loss. For instance, (2.30) and (2.31) result in a term in the IF frequency current of $g_1 \cdot v_{RF}/2$ = $g_{ON} \cdot v_{RF}/\pi$, while the RF frequency current is $g_0 \cdot v_{RF} = g_{ON} \cdot v_{RF}/2$. The ratio of the respective currents is therefore $2/\pi$ so that the conversion gain is $(2/\pi)^2 = 0.41 = -3.92$ dB if the impedances are equal. Because the gain is negative in a passive mixer, we commonly refer to the conversion loss L_C instead, the inverse of (2.35).

The minimum theoretical conversion loss in any passive mixer is 3.92 dB, in which the device is switched with a square wave (i.e., one with a large local-oscillator signal that saturates the device). The loss is invariant to the number of devices in the mixer, since the IF and RF currents will always flow in each device with the same ratio. Of course, any mismatch at the RF port or the IF port will make the conversion loss worse, since the square of the ratio of currents only equals the power ratio when the impedances are equal.

In an ideal mixer, we see from (2.30) and (2.31) that the amplitude of the higher harmonic responses of the LO simply falls as the Fourier coefficients of a square wave. The gain of the IF is -3.92 dB, that of $2\omega_{LO} - \omega_{RF}$ is $(2/3\pi)^2 = -13.5$ dB and that of $3\omega_{LO} - \omega_{RF}$ is $(2/5\pi)^2 = -17.9$ dB. These are the potential spurious responses of the mixer.

In general, the conversion loss will become worse as the LO signal weakens. We can see this from (2.30), because if the LO signal is insufficient to drive the conductance as a square wave, but instead drives it sinusoidally between the same two peak states, then the $g_1 \cdot v_{RF} / 2$ term for the IF frequency component in the output current in (2.31) becomes $g_{ON} \cdot v_{RF} / 4$ (rather than $g_{ON} \cdot v_{RF} / \pi$). The power ratio in (2.35) then becomes 0.25 or -6 dB. As the LO becomes even weaker and is unable to drive the conductance between an off-state and a fully saturated on-state, the peak value of the IF current becomes correspondingly smaller and the conversion loss and noise figure become worse.

Finally, we need to keep in mind that the discussion of conversion gain is with reference to a single-sideband system, for which we translate only one RF component to the IF. Many digital radio systems transmit only the upper or lower sideband of an up-converted signal to preserve spectrum. However, some systems such as analog AM or FM radios use both. In such a double sideband system, then, there will, in fact, be two RF signals that are down-converted to the IF frequency in the receiver, one at $\omega_{RF} = \omega_{LO} - \omega_{IF}$ and the other at $\omega_{RF} = \omega_{LO} + \omega_{IF}$. In that case, the conversion gain and the IF component in (2.31) will be double compared with a single sideband system, where there is only one RF component and a second null sideband, then known as the image frequency. Similarly, the double-sideband noise figure is up to 3 dB improved smaller compared with the single-sideband noise figure, since the IF noise is similar for both mixers but the signal is twice as large for double sideband (DSB) operation.

2.6.2 Noise figure

Noise is generated in mixers by the diode or transistor elements, and by thermal sources due to resistive losses. Noise figures of practical mixers range from $l\sim5$ dB, with diode mixers generally achieving lower noise figures than transistor mixers. The noise figure of a mixer depends on whether its input is a single sideband signal or a double sideband signal. This is because the mixer will converts noise at both sideband frequencies (since these have the same IF), but the power of a SSB signal is one-half that of a DSB signal (for the same amplitude). To derive the relation between the noise figure for these two cases, first consider a DSB input signal of

the form

Upon mixing with an LO signal $cos(\omega_{LO}t)$ and lowpass filtering, the down-converted IF signal will be

where *K* is a constant accounting for the conversion loss for each sideband. The power of the DSB input signal of (2.37) is

For noise figure, the input noise power is defined as $N_i = kT_0B$, where $T_o = 290$ K and B is the IF bandwidth. The output noise power is equal to the input noise plus N_{added} , the noise power added by the mixer, divided by the conversion loss (assuming a reference at the mixer input):

(2.41)

Then using the definition of noise figure gives the DSB noise figure of the mixer as

(2.42)

The corresponding analysis for the SSB case begins with a SSB input signal of the form

(2.43)

(2.45)

Upon mixing with the LO signal $cos(\omega_{LO}t)$ and lowpass filtering, the down-converted IF signal will be

(2.44)

The power of the SSB input signal of (2.43) is

(2.46) The input and output noise powers are the same as for the DSB case, so the noise

figure for the SSB input signal is

and the power of the output IF signal is

(2.47)

Comparison with (2.42) shows that the noise figure of the SSB case is twice of the DSB case

2.6.3 1-dB compression point (P_{1dB})

Like other networks, a mixer is amplitude nonlinearity at a certain input level: above this point, the output level fails to track input level changes proportionally. This figure of merit, P_{1dB} identifies the single tone input signal level at which the output of the mixer has fallen 1 dB below the expected output level.

2.6.4 Dynamic range

The dynamic range of any wireless communication system can be defined as the difference between the 1-dB compression point and the minimum discernible signal (MDS). These two points are specified in units power of the dBm. giving dynamic range in the dB. When the RF input level approaches the 1-dB compression point, harmonic and intermodulation products begin to interfere with the system performance. High dynamic range is obviously desirable, but cost, power consumption, system complexity, and reliability must also be considered.

2.6.5 Intermodulation distortion (IMD)

Nonlinearities in the mixer devices give rise to intermodulation distortion products whenever two or more signals are applied to the mixer's RF port. Testing this behavior with two (usually closely spaced) input signals of equal magnitude can return several figures of merit depending on how the results are interpreted. A mixer's output OIP₃ is defined as the output power level where the spurious signals generated by $(2f_{RF1} \pm f_{RF2}) \pm f_{LO}$ and $(f_{RF1} \pm 2f_{RF2}) \pm f_{LO}$ are equal in amplitude to the desired output signal as shown in Fig. 2.11.

The input third-order intercept point, IIP₃. IP₃ referred to the input level, it is of particularly useful value and is the most commonly used mixer IMR figure of merit. IIP₃ can be calculated according to

 $(\mathbf{0}, \mathbf{1}\mathbf{0})$

where IMR is the intermodulation ratio (the difference in dB between the desired output and the spurious signal), and n is the IM order. The IMD products increase almost exponentially.



Figure 2.11 The mixer linearity evaluation.

2.6.6 LO drive level

A mixer's specifications are usually guaranteed at a particular LO drive level, usually specified as a dBm value that may be qualified with a tolerance. Insufficient LO drive degrades mixer performance. Excessive LO drive degrades performance and may damage mixer devices.

2.6.7 Port isolation

In a mixer, isolation is defined as the attenuation in dB between a signal input at any port and its level as measured at any other port. High isolation numbers are desirable. LO-to-IF and LO-to-RF isolation are dependent mainly on transformer, physical symmetry and device balance, but it is applied to the mixer by level of input signals.

2.6.8 Power consumption

The circuit power consumption is always important. but in battery-powered wireless designs it is critical. The mixer circuit choice may be significant in determining a system's power consumption. The power consumption of the amplifier stage must be considered as well. Evaluating the suitability of a given mixer circuit type requires a grasp of its ecology as well as its specifications.



Chapter 3.

Cascode FET Mixer Design



3.1 Nonlinear FET devices

The GaAs MESFET and its variants, including HEMT, have revolutionized low-noise microwave electronics and microwave systems. FETs also make excellent mixers as they have low-noise levels, broad bandwidths, and conversion gains. As frequency multipliers, they exhibit high efficiency, gain, and output power. FETs are commonly used in quasi-linear applications, especially as small-signal and medium-power amplifiers, where an understanding of their nonlinearities is critical in attractive aspects of their performance, primarily intermodulation distortion and saturation.

The silicon MOSFET technology has progressed to the point where the devices based on it can be used at microwave frequencies. New technologies are making MOSFETs attractive for use in a wide variety of RF applications. Laterally diffused MOSFETs (LDMOS) are attractive for high-power amplifiers at frequencies up to a few gigahertz, and submicron lithography has produced silicon MOSFETS with cut-off frequencies of tens of gigahertz. Interestingly, in spite of their maturity, these devices continue to improve.

Virtually all types of FET devices are highly symmetrical and can be operated with a negative drain-to-source voltage and current. This allows them to be used as resistive elements in switches, attenuators, and mixers.

3.1.1 MESFET operation characteristics

Figure 3.1 shows the cross-section of the GaAs MESFET. MESFET is fabricated by first growing a very pure, semi-insulating buffer layer on a semi-insulating GaAs substrate, then growing an n-doped epitaxial layer that is used to realize the FET's active channel. Three connections are made to the channel: the source and drain ohmic contacts, and between them, the Schottky-barrier gate.



Figure 3.1 The cross-section of the GaAs MESFET.

The epilayer is made thicker than necessary for the channel, and is etched to the correct channel thickness in the gate region. Modern FETs all use a recessed channel with a *T*-shaped gate. The *T*-gate minimizes the gate resistance while retaining a short gate length. This recessed gate structure allows the layer of epitaxial material under the source and drain ohmic contacts to be quite thick, much thicker than the channel, minimizing the parasitic source and drain resistances. Reducing the source resistance is especially important for low-noise devices, and is also important for achieving good conversion efficiency in FET mixers, frequency multipliers, and power amplifiers.

MESFET is biased by the two sources: the V_{ds} of the drain-to-source voltage and the V_{gs} of the gate-to-source voltage. These voltages control the channel current by varying the width of the gate-depletion region and the longitudinal electric field. To acquire a qualitative understanding of MESFET operation, $V_{gs} = 0$ and V_{ds} is raised from zero to some low value, as shown in Fig. 3.2(a). When $V_{gs} = 0$, the depletion region under the Schottky-barrier gate is relatively narrow, and as V_{ds} increases, a longitudinal electric field and a longitudinal electric current are established in the channel.



Figure 3.2 The GaAs MESFET operation (a) very low V_{ds} , (b) V_{ds} at the saturation point, (c) current saturation.

Due to V_{ds} , the voltage across the depletion region is greater at the drain end than at the source end; thus, the depletion region becomes wider at the drain end. The narrowing of the channel and the increased V_{ds} increase the electric field near the drain, which causes the electrons to move faster. Although the channel's conductive cross-section is reduced, the effect is an increased current. When V_{ds} is low, the current is approximately proportional to V_{ds} . If, however, the gate reverse bias is increased while the drain bias is held constant, the depletion region widens, and the conductive channel becomes narrower, which reduces the current. When $V_{gs} = V_t$ (the turn-on or *threshold* voltage), the channel is fully depleted and the drain current is zero, regardless of the value of V_{ds} . In fact, the current does not turn off abruptly, partly because the conductivity of the buffer layer is not zero and the edge of the depletion region is not distinct. Thus, the threshold voltage is somewhat indistinct as well.

It can be defined, for example, as the point where the drain current decreases to some particular fraction of its zero-voltage value. Thus, both V_{gs} and V_{ds} control the drain current. When FET is operated in this manner, it is said to be in its *linear* or *voltage-controlled resistor* region.

If V_{ds} is increased further, as in Fig. 3.2(b), the channel current increases, the depletion region becomes even wider at the drain end, and the conductive channel becomes narrower. Clearly, the current must be constant throughout the channel; thus, as the conductive channel near the drain becomes narrower, the electrons must move faster. The electron velocity cannot increase indefinitely, however, and the average velocity of the electrons in GaAs cannot exceed a velocity called their saturated drift velocity, approximately $1.3 \cdot 10^7$ cm/s. If V_{ds} is increased beyond the value that causes velocity saturation, the electron concentration rather than the velocity must increase to maintain current continuity throughout the channel. Accordingly, a region of electron accumulation forms near the drain end of the gate. Conversely, the electrons transit the channel and move at the saturated velocity into the wide area between the gate and the drain, and an electron depletion region is formed. That depletion region is positively charged because of the positive donor ions remaining in the crystal. As V_{ds} continues to increase, as shown in Fig. 3.2(c), progressively more of the voltage increase is dropped across this region, which is called a *dipole layer*, and less is dropped across the unsaturated part of the channel. Eventually, a point is reached where further increases in V_{ds} are dropped entirely across the charge domain, and where V_{ds} does not substantially increase the drain current. At this point, the electrons move at the saturated drift velocity over a large part of the channel length. When FET is

operated in this manner, which is the normal mode of operation for small-signal devices, it is said to be in its saturation region or in saturated operation. All FET amplifiers and most FET mixers and frequency multipliers are biased into the saturation region. One notable exception is the FET resistive mixer.

It is important to recognize that the charge domain begins to form at drain-to-source voltages well below those corresponding to the horizontal portion of the drain I/V characteristic. Thus, the charge domain affects the I/V characteristic throughout almost the entire range of V_{ds} .

The terms *linear region* and *saturation region* are unfortunate because they seem to indicate exactly the opposite of their true meanings. That is, quasi-linear operation in a small signal takes place in the FET's saturation region and not in its linear region. Further confusion arises because the same terms are used, with opposite meanings, to describe the operating regions of bipolar transistors. That is, a bipolar transistor is said to be in saturation when the collector/emitter voltage is very low.

As in the Schottky-barrier diode, the Schottky-barrier gate depletion region represents a capacitance. At low drain voltages, the gate-to-channel capacitance has nearly the ideal Schottky-barrier voltage dependence, but as V_{ds} increases, the situation becomes more complex. At $V_{ds} \approx 0$, the gate capacitance is distributed along the channel, but it is frequently modeled as two approximately equal capacitors, one between the gate and source and the other between the gate and drain. These capacitances are related to the change in the gate-depletion charge with the changes in gate-to-source voltage V_{gs} and gate-to-drain voltage V_{gd} , respectively.

(3.1)
As V_{ds} is increased and the FET begins saturated operation, however, drain-voltage changes are shielded from the gate depletion region by the dipole layer.

Further changes in V_{ds} no longer increase the charge in the depletion region; thus, the gate-to-drain capacitance drops to a point where it consists of little more than stray capacitance between metallizations. In saturation, the gate-to-source capacitance represents the full gate-depletion capacitance; as such, the gate-to-source capacitance increases to approximately twice its value in linear operation.

3.1.2 HEMT operation

The HEMT differs from a conventional MESFET in that in the former, the channel is formed by a hetero-junction instead of a simple epitaxial layer. As the channel is not doped, impurity scattering is minimized as a high electron mobility result. The mobility increases to decrease the temperature, with substantial improvement in the gain and noise figure, can be achieved at low, even cryogenic, temperatures.



Figure 3.3 The cross-section of the simple AlGaAs-InGaAs-GaAs HEMT.

Figure 3.3 shows a simple HEMT. Instead of a doped epilayer, the device has an n^+ AlGaAs layer and a very thin undoped InGaAs layer immediately underneath it. Due to the band structure of the semiconductors, electrons from the AlGaAs layer accumulate in the InGaAs layer near the interface. Thus, the charge density of this electron layer is controlled by the gate voltage. The charge density is generally very low, making such devices difficult to use as power amplifiers, and to some degree, as frequency multipliers. The high transconductance, however, provides a high cutoff frequency and a very low noise level. These characteristics make HEMTs ideal for low-noise amplifiers and active mixers at frequencies well into the millimeter wave range.

The AlGaAs-InGaAs device is usually called a *pseudomorphic HEMT*, or *pHEMT*, because of the lattice mismatch between the AlGaAs and InGaAs layers. Other types of pHEMTs are possible, as well as devices with multiple hetero-junctions. The latter provide greater channel charge density and thus are useful as power amplifiers. The wide variety of materials, layer thicknesses, and device geometries in the modern HEMT technology provides many degrees of freedom for optimizing the device's channel; in contrast, the only degrees of freedom in the MESFET channel design are thickness and doping density.

The models of HEMTs are not very different from those of MESFETs. One of the greater differences between MESFETs and HEMTs is in the shape of the transconductance curve, as a function of gate voltage. In MESFETs, the transconductance usually increases monotonically with the gate voltage, possibly with a peak at positive V_{gs} ; in HEMTs, it often has a pronounced peak.

3.1.3 MOSFET operation

The operation of MOSFETs has been so thoroughly described in paper that it will be reviewed only briefly here. It is important to note, however, that the advances in the semiconductor technology and submicron lithography have resulted in MOSFETs that are useful at the RF and microwave frequencies. MOS technologies, especially complementary MOS (CMOS), can be very useful, especially for low power, low cost RF ICs.

All RF and microwave devices are enhancement-mode, *n*-channel silicon devices. They consist of a lightly doped *p*-substrate and a gate, either metal or semiconductor, insulated from the substrate by a very thin oxide (SiO₂) layer. At low gate voltages, no channel exists; thus, no conduction is possible. When the gate voltage exceeds a positive threshold voltage, V_t , an inversion layer of electrons is formed under the gate, and that layer acts as a channel. (This is similar in some ways to a HEMT, and in fact, HEMTs have been compared to MOSFETs in terms of their operation.) A simple analysis gives the following expression for the charge density in the channel when $V_d = 0$ and $V_g = V_t$:

where L_g is the gate length, W_g is the gate width, and C_{ox} is the oxide capacitance, the parallel-place capacitance, per area, between the gate and channel. V_d and V_g rather than V_{ds} and V_{gs} are used to represent the internal voltages, which do not include the voltage drop across the source and drain contact resistances R_s and R_d , respectively.

A number of effects can complicate (3.2). One of the most important is called *backgating*, the effect of the voltage between the substrate and the channel, which acts as a kind of second gate. Others are oxide and interface charges, short- and narrow-channel effects, weak inversion (or subthreshold effects), and non-uniform substrate doping.

As in other types of FETs, drain bias application causes the voltage between the gate and the channel to become lower (i.e., more negative) at the drain end. The

charge disappears at the drain end when

and this condition represents the onset of current saturation, much as the completely depleted channel, from a combination of velocity saturation and pinch-off, causes saturation in MESFETs. Velocity saturation, however, plays only a minor role in the operation of silicon devices.

One of the more interesting developments is the laterally diffused MOSFET, or LDMOS, device. It is often used to power amplifiers at giga-hertz.



Figure 3.4 The cross-section of the LDMOS device.

Figure 3.4 shows the cross-section of the LDMOS device. An advantage of this structure is the direct electrical connection of the source to the mounting surface; in contrast, in other power FETs, the drain is connected to the substrate. This eliminates the need for wire bonds or insulators between the chip and the mounting surface, thus minimizing source inductance and resistance.

It also provides better cooling. Other advantages are a low-resistance gate and a long, lightly doped area between the channel and drain contacts, which minimizes

the gate-to-drain capacitance and provides a high breakdown voltage.



3.2 Conventional cascode FET mixer

3.2.1 Design principle of cascode FET mixer

In microwave FET mixers, high gain is usually relatively easy to obtain, but it does not automatically ensure that the other performance aspects will be good. In fact, high mixer gain is often undesirable in receivers because it tends to increase the distortion of the entire receiver. Therefore, in most receiver applications, an active mixer is designed not to achieve the maximum possible conversion gain but to achieve a low noise figure and modest gain, either unity or slightly greater.

The cascode FET mixer consists of two single FETs in series; that is, it has common-source and -gate circuit configuration. It can thus be applied to each gate for inputting at the LO and RF signals. As the capacitance between the gates is low, the mixer will have good LO-to-RF isolation. Due to its high isolation, a cascode FET mixer is composed of two single FETs. Cascode FET mixers are also used in integrated circuits, where filters and distributed-element hybrids may be impractical and where good LO-to-RF isolation may otherwise be difficult to achieve [9-14].

Cascode FET mixers have been successfully used in many kinds of portable and fixed RF receivers for many years. Unfortunately, their reported performance has not been very good, for which reason they are presently not produced in big quantities. Although cascode FET mixers usually exhibit high gain, their noise figures have been disappointing, considerably worse than those of single-FET mixers. One reason for this is that cascode FET mixers have inherent disadvantages compared to single-FET mixers; another is that a cascode FET mixer is a much more complex component than a single-FET mixer, and the subtleties of its operation are not always appreciated by designers. Still, cascode FET mixers have their place, foremost of which is their use in ICs to obtain many of the advantages

of balanced mixers without the need for hybrids.



Figure 3.5 The simplified circuit of cascode FET mixer.

Figure 3.5 shows the simplified circuit of cascode FET mixer. The cascode FET mixer consists of two single-gate FETs in series. The LO is applied to the gate of FET₂, and varies V_{gs2} ; the RF signal is applied to the gate of FET₁. RF and LO sources are connected to gate of FET₁ and gate of FET₂ through external matching circuits, represented by the embedding impedances $Z_{s,RF}(\omega)$ and $Z_{s,LO}(\omega)$, respectively. A series-resonant element (which can be an LC-tuned circuit, a stub, or simply a bypass inductor) is used to ground the gate of FET₂ at the IF frequency. As with the single-gate FET mixer, the load impedance $Z_L(\omega)$ is a short circuit at all LO harmonics and mixing frequencies, except IF; this termination guarantees that the LO power will not be dissipated in the IF load, and that drain voltage V_{ds} will remain constant throughout the LO cycle.

As the cascode FET mixer is the transconductance mixer, mixing must occur by

varying the transconductance between V_{gs1} and I_d . The transconductance variation must be done by varying the drain voltage of FET₁.



Figure 3.6 The *I/V* characteristics of the cascode FET mixer when $V_{ds} = 5.0$ [V].

Figure 3.6 shows the DC drain I/V characteristic of FET₁ in Fig. 3.5 as a function of gate voltages V_{gs1} and V_{gs2} when V_{ds} is fixed at 5.0 V. V_{ds} must be divided between the channels of the two single-gate MESFETs; $V_{ds1} + V_{ds2} = V_{ds}$. When two FETs are connected in series, it is impossible to have a stable operating point if both devices are in current saturation because in this case, the FETs' channels are equivalent to two current sources in series. Inevitably, one device must be saturated, and the other must operate in its linear region. Much of V_{ds} is dropped across the saturated FET.

If FET₂ is linear and FET₁ is saturated (i.e., the operating point is close to the right side of the set of curves in Fig. 3.6), varying V_{gs2} with the LO voltage while V_{gs1} is constant will not vary the transconductance between V_{gs1} and drain current I_d . Therefore, no mixing can occur [15-19].

Significant transconductance variation occurs only when the gate voltages are located within the shaded region of Fig. 3.6, the region in which FET_2 is saturated and FET_1 is linear. In this case, V_{gsl} -to- I_d transconductance variation occurs primarily because the drain voltage of FET_1 is varied from a nearly zero value, which forces the FET_1 to be in its linear region and its channel to have low resistance, and for it to be almost at the point of current saturation.

In a cascode FET mixer, mixing occurs primarily in FET₁; its transconductance and drain-to-source resistance vary with time while the device is in its linear region. In this mode of operation, the peak transconductance of FET₁ is relatively low, and its low drain-to-source resistance shunts the IF output, further reducing the conversion gain. In contrast, a single-FET device is in current saturation throughout the LO cycle; thus, its transconductance is greater and its drain-to-source resistance is very high.

In the cascode FET mixer, FET₂ remains in its saturation region throughout the LO cycle, and its high transconductance varies only moderately. Consequently, FET₂ provides some mixing between the RF drain current of FET₁ and the LO, but its primary effect is to amplify FET₁'s IF output. The series resonator grounds the gate of FET₂, so that FET operates as a common-gate amplifier at the IF frequency. The input impedance of this amplifier is approximately $1/g_{m,avg}(t)$, where $g_{m,avg}(t)$ is the average transconductance of FET₂. As this impedance is usually a mismatch to the IF output impedance of the mixing FET, the amplifier's input coupling is not optimum. As a result, its gain is not great [20-29].

The procedure for designing a cascode FET mixer is much the same as that for designing a single-gate mixer. The cascode FET mixer requires both a carefully designed LO filter at its drain and a resistive IF load. As with a single-gate mixer, the IF output impedance of a cascode FET mixer is relatively high, although for a different reason: the high output impedance is a property of a common-base FET

amplifier. Thus, good gain can be achieved in spite of the inherent limitations of the device, by using a relatively high IF load resistance value. The IF resonator connected to the gate of FET₂ critically affects the mixer's stability and LO efficiency. If the resonator's reactance at the LO frequency is too low, the LO matching may be poor; at some frequency, however, the combination of the resonator's reactance and the impedance of $Z_{s,LO}(\omega)$ may cause the mixer to oscillate. One can avoid such problems by making sure that $Z_{s,LO}(\omega)$ and the resonator do not present a high inductive reactance to the gate of FET₂ outside the LO frequency range. As with a single-FET mixer, source and load impedances $Z_{s,RF}(\omega)$ and $Z_L(\omega)$ should be short circuits at unwanted mixing frequencies.

3.2.2 Approximate small-signal analysis of cascode FET mixer

Figure 3.7 shows the approximate small-signal equivalent circuit of cascode FET mixer using common-source and –gate configuration.



Figure 3.7 The simplified small-signal equivalent circuit of the cascode FET mixer.

The fundamental frequency of $g_{m1}(t)$ and $g_{m2}(t)$, such as that in (3.4), are dominant in providing conventional down-conversion mixing.

The IF current gives

(3.5)

where $v_{ds}(t)$ is the small-signal drain-to-source voltage of the FET₂ device. Substituting (3.4) into (3.5) and separating the IF component will give

It was noted that $v_{ds} \approx g_{m1} \cdot v_{g1} / R_{d2}$; thus, the second term is smaller than the first by a factor of at least R_{ds1} / R_{d2} . In fact, it is smaller than this because of the loading effect of C_{gs2} and R_{s2} . (R_{g1} is the sum of the source, intrinsic, and gate resistances of the FET₁ device). Thus, the second term in (3.6) is usually negligible, and only $g_{m1}(t)$ provides significant mixing. If the input is conjugate-matched, the following can be obtained:

Similarly, it was assumed that g_{ds2} is negligible ($g_{ds2} \ll Re\{Z_L(\omega_0)\}$) and that the

load susceptance resonates C_{ds2} . Note that g_{m2} is time-invariant. Finally, the conversion gain is for $R_{d2} = R_L$ and $R_{g1} = R_{in}$, and the transconductance waveform is a half sinusoid, $g_{m1,max} = G_{m,max}/4$, thus representing

In the above equations, it was already noted that g_{ml} in the cascode FET device is lower than that in a single-FET device, and consequently, that the conversion gain of the cascode FET mixer is significantly lower than that of a single-FET mixer.

Although the noise and conversion efficiency of cascode FET mixers are generally worse than those of single-gate mixers, the intermodulation characteristics are often moderate. The drain current as a function of gate voltage V_{gs1} is usually more linear in a cascode FET mixer than in a single-FET device [30-35].

3.3 Cascode FET mixer using new circuit configuration

3.3.1 Design principle of cascode FET mixer using new circuit configuration

Figure 3.8 shows the simplified circuit of the cascode FET mixer using new common-source and -drain circuit configuration. As shown in the Fig. 3.8, it consists of the same configuration as that of the conventional cascode FET mixer.



Figure 3.8 The simplified circuit of the cascode FET mixer using new common-source and -drain circuit configuration.

The output port of the IF frequency, however, is between the drain of FET_1 and the source of FET_2 , and the other type of mixer has not yet been reported as the proposed cascode FET mixer using new circuit configuration. Most active FET mixers have the LO and RF signals applied to each gate and the IF filtered from the drain. The matching circuit of the cascode FET mixer using new circuit configuration consists of RF, LO, and IF matching circuits. The matching circuits provide filtering as well as matching; they terminate the FET's gate and drain at unwanted frequencies (mixing products and LO harmonics) and provide port-to-port isolation.

The time-varying transconductance is the dominant contributor to frequency conversion. In such cascode FET mixer, the effects of harmonically varying the gate-to-drain capacitance, gate-to-source capacitance, and drain-to-source resistance are often deleterious and must thus be minimized. As the time-varying transconductance is the primary contributor to mixing, it is important to maximize the range of the FET's transconductance variation. In simple down-converters, they are most concerned with the magnitude of the fundamental frequency component of the transconductance.



Figure 3.9 The I/V characteristic of the cascode FET mixer when $V_{ds} = 5.0$ [V]. (I) is high-linearity region, (II) is high-conversion region.

Figure 3.9 shows the I/V characteristic of the cascode FET mixer, where (I) is

high-linearity region and (II) is high-conversion region. To maximize the fundamental frequency component of the transconductance variation, FET₂ must be biased close to its threshold voltage, V_t , and must remain in its current saturation region throughout the LO cycle. Full saturation can be achieved by drain voltage V_{DD} if the LO pumping will be maintained under the DC value of V_{DD} . This condition can be achieved by short-circuiting the drain of FET₂ at the fundamental LO frequency and in all LO harmonics. If the drain is effectively shorted, the drain LO current will operate seemingly as a switching circuit, which may have a fairly high peak value and cannot cause any drain-to-source voltage variation. As such, the LO voltage across the gate-to-drain capacitance will be minimal, and for this reason, the feedback of the LO voltage will also be minimal, and the mixer will be stable. In this case, the drain current will have the same half-sinusoidal pulse waveform as a class-B power amplifier, and the transconductance waveform will be similar. Thus, the source current of FET₂ will be similar to the drain current of FET_1 . The drain current of FET_2 will be provided with the necessary current in the drain of FET_1 through the source of FET_2 , as shown in Fig. 3.8.

For the gate voltage of FET_1 , the bias voltage of the gate for high transconductance must be set up at a high-conversion gain region because FET_1 makes up a large part of the frequency harmonic component and conversion gain, which is called *transconductance stage*. The drain voltage of FET_1 is maximized to bias the same drain voltage that will be used in an amplifier. For high performance, the gate voltage of FET_1 must adjust the bias point between the triode region and the saturation region. For the operation into the triode region, it is more important to have high linearity than high conversion gain while for the operation into the saturation region, the opposite is true. Thus, the performance of the cascade FET mixer is usually insensitive to small changes in the DC drain voltage, but it is sensitive to the DC gate voltage, which must be made a steady rippleless voltage

via circuit tuning.

With the cascode FET mixer using new circuit configuration, it is possible to find each input and output impedance between the drain of FET₁ and the source of FET₂ for impedance matching, which is the simultaneous matching of the RF input, LO input, and IF output ports, such as in the conventional cascode FET mixer. This is impossible, however, with the conventional cascode FET mixer as its load impedance is very high. If the mixer is unconditionally stable, the output impedance of FET₂ at below 10 GHz down-converter will be very high, and its resistive part will be much greater than the drain-to-source resistance of a DC-biased FET_1 . To obtain a conjugate-matched to such a high impedance, it is sometimes impossible to match the IF output of an active FET mixer. A better method is to use a resistive load at the IF port, whose value is selected to obtain the desired conversion gain. In this case, the active mixer's output reflection coefficient is high-impedance, but the theoretical and practical limitations of impedance matching are such that the unmatched output reflection coefficient is unavoidable. If the resistive load is properly implemented, the conventional cascode FET mixer will provide stable operation, a flat frequency response, and the desired gain. It does not matter, however, if the conventional cascode FET mixer has an IF port at the drain of FET₂ because the cascode FET mixer using new circuit configuration has no output IF port at the drain of FET₂. Moreover, having a drain in FET₁ and a source in FET₂, the cascode FET mixer using new circuit configuration can achieve easily impedance matching at the IF port.

Ordinary small-signal HEMTs and MESFETs are used to manufacture mixers. A FET designed to be used in low-noise amplifiers within a specific frequency range usually works well as a mixer within the same range. Special situations often affect the choice of a device. For example, it is generally easier to obtain a high intermodulation intercept point from a device with a relatively wide gate, and there is some experimental evidence that good noise figure can be more readily obtained by using narrow devices. Most millimeter-wave devices are optimized for amplifier use and therefore have very narrow gates.

For the LO-to-IF isolation characteristic, in the conventional cascode FET mixer, achieving adequate LO-to-IF isolation can be difficult in active mixers. If the LO is really short-circuited at the drain, there can be no LO leakage when using a $\lambda/4$ open-stub circuit for the LO frequency. As the short circuit, however, is never perfect, some degree of leakage is inevitable. The LO current in the conventional cascode FET's drain is very great, its peak value is somewhat above *I*_{dss}, and even in small-signal devices, it may be over 100 mA. Consequently, the output power in the LO frequency is potentially very high.

The cascode FET mixer using new circuit configuration, however, has a higher LO-to-IF isolation characteristic than the conventional one because due to the R_d of FET₁ and the R_s of FET₂, the R_s of FET₂ is higher than the R_d of FET₂. Accordingly, the LO-to-IF isolation of the cascode FET mixer using new circuit configuration has no influence on the conversion gain and on the spurious responses at the IF output port.

Unfortunately, it is difficult to design an IF matching circuit in the conventional cascode FET mixer that provides high LO isolation and that still meets all the other requirements. Therefore, even in well-designed mixers, the level of LO leakage from the IF port is often high, sometimes even higher than the applied LO power. This LO leakage can saturate the IF amplifier or can generate spurious signals. Accordingly, it is important for the IF output circuit to include sufficient filtering so that adequate LO-to-IF isolation can be provided. The required rejection depends on the FET's output power capability and the level of LO leakage that the IF amplifier can tolerate.

It is, however, easy to design an IF output matching circuit in the cascode FET

mixer using new circuit configuration. Moreover, it is easy to achieve an IF output matching circuit for FET_1 through the impedance between the drain of FET_1 and the source of FET_2 , and it is not a concern that it will generate spurious signals because of the LO frequency and level compared with the conventional one. Thus, most conventional cascode FET mixers have LO rejection filters so as to reject LO leakage in the IF output. The cascode FET mixer using new circuit configuration, however, does not need a LO rejection filter because of its advantage of using impedance.

3.3.2 Approximate small-signal analysis of cascode FET mixer using novel configuration

Approximated small-signal analysis of the proposed cascode FET mixer using new circuit configuration is shown herein.



Figure 3.10 The simplified equivalent circuit of the cascode FET mixer using new circuit configuration.

It is possible to simplify the FET equivalent circuit to obtain the approximately

equivalent circuit shown in Fig. 3.10.

The design of a cascode FET mixer using new circuit configuration must optimize the large-signal LO pumping as well as the small-signal operation. For the design at the gate of FET₂ with the LO, it is considered that FET₂ must be short-circuited at the source at the LO fundamental frequency and at the gate in all the harmonics, except at the fundamental frequency. FET₂ achieves a configuration in which it serves as the common-drain amplifier, as shown in Fig. 3.10. Its operation characteristic is that the input signal is applied to the gate and the output is taken as the source. The output voltage is equal to the input voltage minus the gate-source voltage. Thus, the resulting output voltage is simply offset from the input, and the small-signal gain would be unity. Therefore, the source follows the gate, and the circuit is called *source follower*.

This is shown by the effects of the small-signal analysis. The small-signal equivalent circuit assumes that FET_2 is connected to FET_1 . V_{GS2} is the gate-source DC voltage of FET_2 , which is given by

The V_{GS2} shows the correlation between the input signal voltage of $v_{in2}(t)$ and the output signal voltage of $v_{out2}(t)$. $v_{out2}(t)$ is given by

(3.11)

The $g_{m2}(t)$ of FET₂ represents the output voltage gain due to the increase in V_{GS2} . In equation (3.11), $i_{d2}(t)$ is the drain current of FET₂, which is rearranged as

The $i_{d2}(t)$ shows the correlation between the transconductance $g_{m2}(t)$ of FET₂ and

the gate-source DC voltage of $V_{GS2}(t)$, which shows a high current transfer characteristic due to the increase in the $g_{m2}(t)$ of FET₂. V_{GS2} is rearranged in another way by (3.11), given by

The V_{GS2} shows the correlation between the input signal voltage of $v_{in2}(t)$ and the drain current of $i_{d2}(t)$. In equation (3.13), $i_{d2}(t)$ is rearranged as in (3.12).

The $i_{d2}(t)$ shows the correlation between input signal $v_{m2}(t)$ of FET₂ and gate-source DC voltage $V_{GS2}(t)$, which shows a high current transfer characteristic due to the high input signal voltage $v_{m2}(t)$ of FET₂.

In equations (3.12) and (3.14), the drain current of FET₂ consists of an effective current transfer characteristic due to the control of the input signal voltage $v_{m2}(t)$ and transconductance $g_{m2}(t)$ as well as the gate-source DC voltage V_{GS2} of FET₂. It is an important current characteristic for the drain current of FET₁. Drain current $i_{d2}(t)$ is shown to have an effective drain current gain in (3.12) and (3.14).

As shown in (3.12) and (3.14), $i_{d2}(t)$ is represented as

The drain current of FET_2 is like the source current of FET_1 , and the source current of FET_2 is like the drain current of FET_1 .

The LO input matching circuit can be estimated from the assumption that the input reflection coefficient is conjugate-matched, $R_{in2} = R_{g2} + R_{s2} + R_{i2}$. It is assumed that the gate of FET₂ is biased at bias voltage V_{GG2} , and that the LO voltage at the gate of FET₂ varies between $V_{g2,max}$ (the maximum forward gate

voltage, limited by the gate-to-channel rectification in the pHEMTs at $V_{g2,max} \approx 0.5$ V) and the maximum reverse voltage of $2 \cdot V_t - V_{g2,max}$, where $\omega = \omega_p$ is the LO frequency. In generating this circuit, C_{gd2} is effectively parallel with C_{gs2} . Usually, $C_{gd2} \ll C_{gs2}$; thus, C_{gd2} can be neglected. The output port of FET₁ is tuned onto the IF frequency, and each tuned input circuit of FET₁ and FET₂ are made matching circuits by the RF and LO frequencies. The LO power is

If the gate of FET₂ is not conjugate-matched at the LO frequency, the reflection losses must be included.

If the transconductance waveform can be approximated by the pulse train of the half-sinusoids shown in the source of FET₂, the FET₁ in Fig. 3.10 can be analyzed relatively to determine its conversion gain. The input impedance at the gate of FET₂ is not highly sensitive to the signal level, which is not driven to the point of rectification in the gate, and the expression for the input impedance at the gate of FET₁ is the same as the LO input impedance at the gate of FET₂.

FET₁ achieves a configuration in which it is well known as serving as a common-source amplifier, as shown in Fig. 3.10. Its operation characteristic is that the input signal is applied to the gate and the output is taken from the drain. The input impedance of FET₁, as shown in Fig. 3.10, is

where C_{gsl} is the gate-to-source capacitance of FET₁ at the bias voltage $V_{GSl} = g_{ml}(t)$ (in Fig. 3.9, a high-conversion region), and $R_{in,l}$ is the resistance of FET₁ in the input loop. In a MESFET or pHEMT, $R_{inl} = R_{gl} + R_{sl} + R_{il}$ is the sum of the gate, source, and intrinsic resistances. Ideally, the input-matching circuit should

match the input impedance of FET_1 at the RF frequency. In this case, the RF frequency is significantly important, and it is possible to match the device successfully at the RF frequency. A poor RF match will degrade the conversion performance.

The RF input of FET₁ is usually conjugate-matched, as is likely with amplifiers, but it is not clear if similar techniques will improve the noise level of the mixer. The current $i_{in1}(t)$ of the RF excitation is expressed as

where ω_l is the RF frequency. If the source is matched, $Z_{Gl}(\omega_l) = Z_{Gl} * (\omega_l)$, and the small-signal gate voltage will be

altille .

The phase shift φ will not be evaluated herein because it does not affect the conversion gain. The fundamental-frequency component of $g_{ml}(t)$ is

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where $g_{m1,max}$ is the peak value of $g_{m1}(t)$. The small-signal drain current $i_{d1}(t)$ is given by

(3.21)

The current $i_{d1}(t)$ includes the components at the RF and IF frequencies and at all other mixing frequencies and all harmonics. Substituting (3.19) and (3.20) into (3.21), employing the usual trigonometric identities, and retaining only the terms at the IF frequency will give the IF component of $i_{d1}(t)$ and $i_{IF}(t)$. Note that only the fundamental component $g_{m1}(t)$ of $g_m(t)$ contributes to frequency conversion, as

where ω_0 is the IF frequency. The IF output power is

(3.23)

The available power from the conjugate-matched source is

(3.24)

and the transducer conversion gain is G_t , comprising the ratio of (3.23) and (3.24)

Equation (3.25) is remarkably accurate as long as the optimum impedances are achieved and the gate of FET₁ is optimally biased. Equation (3.25) seems to imply that it is possible to achieve high conversion gain by increasing IF load impedance R_L or by increasing the device's width owing to the increasing $g_{m1,max}$. These implications are generally valid, but practical difficulties limit the conversion gain. Problems involving stability and realizability limit the R_L of high impedances, and the FET's output capacitance limits the bandwidth if R_L is made too large. If the device width is overly increased, the resulting decrease in input impedance will be a difficult matching circuit. The cascode FET mixer design is relatively important as it should estimate the important parameters of the $g_{m,max}$, R_{in} , and $C_{gs}(t)$ of FET. The peak transconductance $g_{m,max}$ can be found from the DC simulation as the

resistance C_{gs} can be estimated with adequate accuracy from the FET's S-parameters. The value of R_L is determined by the gain requirement, as indicated in (3.25), and the input impedance can be estimated using (3.17).



Chapter 4.

Simulation and Measurement Results



4.1 Comparison of simulation results

For the verification of the RF performance of the cascode FET mixer using new circuit configuration, the simulation results for the cascode FET mixer using new common-source and -drain circuit configuration and for the conventional cascode FET mixer are exhibited herein.

For the active device, the ATF-36163 model of Avago Technologies, a low-noise pHEMT, was used. It has a nominal gate length of 0.2 μ m and a total gate width of 200 μ m. The gold-based metallization system and nitride passivation have been proven to be rugged devices. For the substrate for the circuit layout, the ORCER RF-35 substrate of Taconic's dielectric, an organic-ceramic laminate, was used. It is based on a woven glass reinforcement and has a thickness of 0.76 mm, a copper thickness of 35 μ m, a dielectric constant of 3.5, and a dissipation factor of 0.0018. The RF design tool that was used for the simulation was the ADS that had been realized by Agilent Technologies EEsoft.

Figure 4.1 is a schematic for the designed conventional cascode FET mixer, which was designed as the well-known cascode FET mixer with the characteristics of high conversion gain, high linearity, low noise level, and poor LO-to-IF isolation. The conventional cascode FET mixer in Fig. 4.1 was designed to have high conversion gain and high linearity for comparison of the cascode FET mixer using new circuit configuration.



Figure 4.1 A schematic for designed conventional cascode FET mixer.



Figure 4.2 A schematic for cascode FET mixer using new common-source and -drain circuit configuration.

Figure 4.2 is a schematic for the cascode FET mixer using new common-source and -drain circuit configuration, whose IF output port had a location different from that in the conventional cascode FET mixer. The cascode FET mixer using new circuit configuration was expected to show enhanced RF performance because the new circuit configuration had common-source and -drain, and its RF performance parameter values were expected to be comparable to those of the conventional cascode FET mixer.

All the circuits were performed with an RF frequency of 2.6 GHz, an LO frequency of 2.5 GHz, and an IF frequency of 100 MHz, and the DC-block and DC-feed circuits had a chip capacitance of 100 pF and a chip inductance of 100 nH, respectively.



Figure 4.3 The simulated I/V characteristic of FET₁ in the conventional cascode FET mixer.

Figure 4.3 shows the simulated I/V characteristic of FET₁ in the conventional cascode FET mixer in Fig. 4.1. In Fig. 4.3, the drain current was decided as a function of gate voltage V_{gs1} when V_{dd} was fixed at 2.0 V. The gate voltage was set at -0.02 V, which is the operation point with a high conversion region for high transconductance, as shown in the shaded area in Fig. 3.6. When gate voltage V_{gs1}

was -0.02 V, drain current I_{ds} was 9 mA, and the DC power consumption was 18 mW. Under these conditions, the cascode FET mixer using new circuit configuration is necessary to have the same power consumption. FET₂ shows a biased gate voltage V_{gs2} of -0.08 V, which is the operation point for performing as a pumping circuit by LO frequency level. If gate voltage V_{gs2} is in the near-zero region, the amplified LO signal with all the LO harmonics and its mixing frequencies will influence the IF port of the wanted signals and will become an unstable mixer circuit due to its generation of unnecessary LO harmonics, and it can have worse effects on the LO-to-IF isolation characteristic. Therefore, gate voltage V_{gs2} was set below the zero region and is fully considered for its various effects.



Figure 4.4 The simulated I/V characteristic of FET₁ in the cascode FET mixer using new circuit configuration.

Figure 4.4 shows the simulated I/V characteristic of FET₁ in the cascode FET mixer using new circuit configuration, as shown in Fig. 4.2. The drain current was decided as a function of gate voltage V_{gs1} when V_{dd} was fixed at 2.0 V. Gate voltage V_{gs1} was set at -0.08 V, which is a stable operation point for the high-linearity and high-conversion region, as shown in Fig. 3.9. When gate voltage V_{gs1} was -0.02 V,

drain current I_{ds} was 9 mA, and the DC power consumption was 18 mW. FET₁ with the decided gate voltage V_{gs1} performed as a class-A amplifier or as a maximum available gain amplifier to produce a ratio of input and output power. FET₂ shows a biased gate voltage V_{gs2} of -0.02 V, which is a stable operation point for performing as a pumping circuit by LO frequency level. It was approximated as the current saturation region.



Figure 4.5 The comparison of simulated conversion gain characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer.

Figure 4.5 shows the comparison of the simulated conversion gain characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. The simulated conversion gain was a function of LO power, as shown in Fig. 4.5. The conventional cascode FET mixer showed maximum conversion gain of 7.15 dB when LO power was 2 dBm and RF power was -40 dBm. The cascode FET mixer using new circuit configuration, on the other hand, showed maximum conversion gain of 11.74 dB when LO power was -4 dBm and RF power was -40 dBm. These results show a difference between the two mixers,

with the proposed cascade FET mixer using new circuit configuration having higher conversion gain of 4.59 dB compared with the conventional cascode FET mixer. The cascode FET mixer using new circuit configuration showed high conversion gain with lower LO power, as opposed to the conventional cascode FET mixer. The proposed mixer does not need local oscillator circuit with large output power as it needs lower input LO power compared with the conventional cascode FET mixer. This is an important characteristic for the effective power consumption of the wireless communication system.



Figure 4.6 The comparison of simulated LO-to-IF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer.

Figure 4.6 shows the comparison of simulated LO-to-IF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. The simulated LO-to-IF isolation characteristic was a function of LO power, as shown in Fig. 4.6. The conventional cascode FET mixer showed LO-to-IF isolation characteristic of -7.56 dBm when the maximum conversion gain was 7.15 dB at LO power of 2 dBm and RF power of -40 dBm. The cascode FET

mixer using new circuit configuration showed LO-to-IF isolation characteristic of -40.64 dBm when the maximum conversion gain was 11.74 dB at LO power of -4 dBm and RF power of -40 dBm. These results show a difference between the two mixers, with the proposed mixer having very high LO-to-IF isolation characteristic of 33.08 dB compared with the conventional cascode FET mixer. The proposed cascode FET mixer using new circuit configuration thus has very high LO-to-IF isolation than the conventional cascode FET mixer.



Figure 4.7 The comparison of simulated LO-to-RF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer.

Figure 4.7 shows the comparison of simulated LO-to-RF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. The simulated LO-to-RF isolation characteristic was a function of LO power, as shown in Fig. 4.7. The conventional cascode FET mixer showed LO-to-RF isolation characteristic of -17.79 dBm when the maximum conversion gain was 7.15 dB at LO power of 2 dBm and RF power of -40 dBm. The cascode FET mixer using new circuit configuration, on the other hand, showed

LO-to-RF isolation characteristic of -25.4 dBm when the maximum conversion gain was 11.74 dB at LO power of -4 dBm and RF power of -40 dBm. These results show a difference between the two mixers, with the proposed mixer having high LO-to-RF isolation characteristic of 7.61 dB compared with the conventional cascode FET mixer. The cascode FET mixer using new circuit configuration thus showed better LO-to-RF isolation than the conventional cascode FET mixer.



Figure 4.8 The comparison of simulated noise figure characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer.

Figure 4.8 shows the comparison of simulated noise figure characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. The simulated noise figure characteristic was a function of LO power, as shown in Fig. 4.8. For the ambient and nominal temperatures of the active-device model for the simulation, 16.85 and 25°C were used, respectively. The conventional cascode FET mixer showed minimum noise figure characteristic of 9.31 dB when the conversion gain was 7.15 dB at LO power of 3 dBm and RF power of -40 dBm. The cascode FET mixer using new circuit configuration, on the

other hand, showed noise figure characteristic of 4.34 dB when the conversion gain was 10.67 dB at LO power of -2 dBm and RF power of -40 dBm.

These results show a difference between the two mixers, with the proposed mixer having lower noise figure of 4.97 dB compared with the conventional cascode FET mixer. The cascode FET mixer using new circuit configuration thus showed very low noise figure than the conventional cascode FET mixer. This is due to the use only of the g_{ml} of FET₁, which has an effect on the noise figure characteristic because of the nonlinearity of the active device.



Figure 4.9 The simulated P_{1dB} characteristic of the conventional cascode FET mixer.

Figure 4.9 shows the simulated P_{1dB} characteristic of the conventional cascode FET mixer. The simulated P_{1dB} characteristic was a function of RF power, as shown in Fig. 4.9. The conventional cascode FET mixer showed P_{1dB} characteristic in which the input RF and output IF power were -8.0 and -5.33 dBm, respectively. This was the operation condition when the conversion gain was 3.23 dB at LO power of -3 dBm and RF power of -40 dBm.

Figure 4.10 shows the simulated P_{1dB} characteristic of the cascode FET mixer

using new circuit configuration.



Figure 4.10 The simulated P_{1dB} characteristic of the cascode FET mixer using new circuit configuration.

The simulated P_{1dB} characteristic was a function of RF power, as shown in Fig. 4.10. The cascode FET mixer using new circuit configuration showed P_{1dB} characteristic in which the input RF and output IF power were -18.0 dBm and -15.62 dBm, respectively. This was the operation condition when the conversion gain was 3.38 dB at LO power of -13 dBm and RF power of -40 dBm. In the results shown in Fig. 4.9 and 4.10, a difference can be observed between the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer, which had a low output IF power of 10.29 dB under the same conditions as when a conversion gain of about 3 dB was attained.

Figure 4.11 shows the simulated IP₃ characteristic of the LSB using two tones for the conventional cascode FET mixer. The simulated IP₃ characteristic was a function of RF power, as shown in Fig. 4.11. The conventional cascode FET mixer showed the IP₃ characteristic of the LSB with an RF frequency of 2.599 GHz where the IIP₃ and OIP₃ were -11.64 and -8.05 dBm, respectively. This was the condition when the conversion gain was 3.17 dB at IF frequency of 99 MHz at LO power of -3 dBm and RF power of -40 dBm.



Figure 4.11 The simulated IP₃ characteristic of LSB using two-tones for the conventional cascode FET mixer.



Figure 4.12 The simulated IP₃ characteristic of USB using two-tones for the conventional cascode FET mixer.

Figure 4.12 shows the simulated IP_3 characteristic of the USB using two tones for the conventional cascode FET mixer. The simulated IP_3 characteristic was a
function of RF power, as shown in Fig. 4.12. The conventional cascode FET mixer showed the IP₃ characteristic of the USB with RF frequency of 2.601 GHz where the IIP₃ and OIP₃ were -1.33 and 2.79 dBm, respectively. This was the condition when the conversion gain was 3.69 dB at IF frequency of 101 MHz at LO power of -3 dBm and RF power of -40 dBm.



Figure 4.13 The simulated IP₃ characteristic of LSB using two-tones for the cascode FET mixer using new circuit configuration.

Figure 4.13 shows the simulated IP₃ characteristic of the LSB using two tones for the cascode FET mixer using new circuit configuration. The simulated IP₃ characteristic was a function of RF power, as shown in Fig. 4.13. The cascode FET mixer using new circuit configuration showed the IP₃ characteristic of the LSB with RF frequency of 2.599 GHz where the IIP₃ and OIP₃ were -17.96 and -14.18 dBm, respectively. This was the condition when the conversion gain was 3.78 dB at IF frequency of 99 MHz at LO power of -13 dBm and RF power of -40 dBm.

The results shown in Fig. 4.11 and 4.13 showed a difference between the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer, which had input RF power of -6.32 dBm for the LSB under the same

simulation conditions. The cascode FET mixer using new circuit configuration showed low linearity than the conventional cascode FET mixer. It saturated the g_{mI} of FET₁ because of its high gain characteristic.



Figure 4.14 The simulated IP₃ characteristic of USB using two-tones for the cascode FET mixer using new circuit configuration.

Figure 4.14 shows the simulated IP₃ characteristic of the USB using two tones for the cascode FET mixer using new circuit configuration. The simulated IP₃ characteristic was a function of RF power, as shown in Fig. 4.14. The cascode FET mixer using new circuit configuration showed the IP₃ characteristic of the USB with RF frequency of 2.601 GHz where the IIP₃ and OIP₃ were -13.76 and -10.02 dBm, respectively. This was the condition when the conversion gain was 3.74 dB at IF frequency of 101 MHz at LO power of -13 dBm and RF power of -40 dBm.

The results shown in Fig. 4.12 and 4.14 showed a difference between the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer, which had input RF power USB of -12.43 dBm under the same simulation conditions. The cascode FET mixer using new circuit configuration showed low linearity than the conventional cascode FET mixer. It also saturated

the g_{m1} of FET₁ because of its high gain characteristic.



Figure 4.15 The simulated IF output power spectrum using two-tones for the conventional cascode FET mixer.

Figure 4.15 shows the simulated IF output power spectrum using two tones for the conventional cascode FET mixer. Figure 4.15 shows the simulation conditions when the LO power was -3 dBm and the RF power was -40 dBm. The conventional cascode FET mixer for the LSB showed output IF power of -36.83 dBm at the fundamental IF frequency of 99 MHz, and output IF power of -94.38 dBm at the third-order intermodulation IF frequency of 97 MHz. Further, it had a conversion gain of 3.17 dB at the LSB with RF frequency of 2.599 GHz. The conventional cascode FET mixer for the USB showed output IF power of -36.31 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -114.5 dBm at the fundamental IF frequency of 2.601 GHz.

The results showed that the intermodulation distortion for the LSB and USB were 57.56 dB at the RF frequency of 2.599 GHz and 78.19 dB at the RF frequency of 2.601 GHz, respectively.



Figure 4.16 The simulated IF output power spectrum using two-tones for the cascode FET mixer using new circuit configuration.

Figure 4.16 shows the simulated IF output power spectrum using two tones for the cascode FET mixer using new circuit configuration. Figure 4.16 shows the simulation conditions when the LO power was -13 dBm and the RF power was -40 dBm. The cascode FET mixer using new circuit configuration for the LSB showed output IF power of -36.22 dBm at the fundamental IF frequency of 99 MHz, and output IF power of -80.31 dBm at the third-order intermodulation IF frequency of 97 MHz. Further, it had a conversion gain of 3.78 dB at the LSB with RF frequency of 2.599 GHz. The cascode FET mixer using new circuit configuration for the USB showed output IF power of -36.26 dBm at the fundamental IF frequency of 101 MHz, and output IF power of -88.75 dBm at the third-order intermodulation IF frequency of 2.601 GHz.

The results showed that the intermodulation distortion for the LSB and USB were 40.09 dB at the RF frequency of 2.599 GHz and 52.48 dB at the RF frequency of 2.601 GHz, respectively.

In the results shown in Fig. 4.16 and 4.17, a difference was shown between the

cascode FET mixer using new circuit configuration and the conventional cascode FET mixer, which had LSB intermodulation distortion of 13.47 dB and USB intermodulation distortion of 25.71 dB. The cascode FET mixer using new circuit configuration showed low LSB and USB intermodulation distortion because of its higher conversion gain characteristic compared with the conventional cascode FET mixer.



Figure 4.17 The simulated reflection coefficient characteristics of S_{11} , S_{22} and S_{33} for the conventional cascode FET mixer.

Figure 4.17 shows the simulated reflection coefficient characteristics of S_{11} , S_{22} , and S_{33} for the conventional cascode FET mixer. In Fig. 4.17, the values of such characteristics matched the matching circuit at the LO frequency of 2.5 GHz, the RF frequency of 2.6 GHz, and the IF frequency of 100 MHz. The simulated reflection coefficient characteristics of the conventional cascode FET mixer showed the S_{11} of -28.4 dB at the LO frequency, the S_{22} of -31.05 dB at the RF frequency, and the S_{33} of -22.01 dB at the IF frequency.

Figure 4.18 shows the simulated reflection coefficient characteristics of S_{11} , S_{22} , and S_{33} for the cascode FET mixer using new circuit configuration.



Figure 4.18 The simulated reflection coefficient characteristics of S_{11} , S_{22} and S_{33} for the cascode FET mixer using new circuit configuration.

In Fig. 4.18, the values of such characteristics also matched the matching circuit at the LO frequency of 2.5 GHz, the RF frequency of 2.6 GHz, and the IF frequency of 100 MHz. The simulated reflection coefficient characteristics of the cascode FET mixer using new circuit configuration showed the S_{11} of -29.13 dB at the LO frequency, the S_{22} of -29.22 dB at the RF frequency, and the S_{33} of -29.11 dB at the IF frequency.

Table 4.1 is a summary of the RF performance simulation results for the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. It compares the RF performance simulation results of the two mixers.

Table 4.1 The summary of the RF performance simulation results for the cascodeFET mixer using new circuit configuration and the conventionalcascode FET mixer.

	The proposed cascode	The conventional
Characteristic	FET mixer	cascode FET mixer
DC power consumption [mW]	9.0	9.0
Max. conversion gain [dB]	11.74	7.15
	(at LO power = -4)	(at LO power=+2)
LO-to-IF isolation [dBm]	-49.31	-9.67
	(at LO power = -13)	(at LO power = -3)
LO-to-RF isolation [dBm]	-35.24	-22.77
	(at LO power $=$ -13)	(at LO power $=$ -3)
Min. noise figure [dB]	4.34	9.31
	(at LO power = -2)	(at LO power = $+3$)
P _{1dB} [dBm]	-15.62	-5.33
	(at RF power = -18)	(at RF power = -8)
	(at LO power = -13)	(at LO power = -3)
IP ₃ of LSB [dBm]	IIP3 = -17.96	IIP3 = -11.64
	OIP3 = -14.18	OIP3 = -8.05
	(at LO power $=$ -13)	(at LO power $=$ -3)
IP3 of USB [dBm]	IIP3 = -13.76	IIP3 = -1.33
	OIP3 = -10.02	OIP3 = +2.79
	(at LO power = -13)	(at LO power = -3)
IMD [dB]	LSB = 44.09	LSB = 57.56
	USB = 52.48	USB = 78.19
Reflection coefficient [dB]	$S_{11} = -29.13$	$S_{11} = -28.4$
	$S_{22} = -29.22$	$S_{22} = -31.05$
	$S_{33} = -29.11$	$S_{33} = -22.01$

4.2 Comparison of measurement results

For the verification of the RF performance simulation results of the cascode FET mixer using new circuit configuration, the measurement results for the cascode FET mixer using new circuit configuration and for the conventional cascode FET mixer are exhibited herein.

The cascode FET mixer using new circuit configuration and the conventional cascode FET mixer were fabricated on a printed substrate. The active device that was used was the ATF-36163 model of Avago Technologies, which is a low-noise pHEMT with a nominal gate length of 0.2 μ m and a total gate width of 200 μ m. The substrate that was used for the circuit layout was the ORCER RF-35 model of Taconic's dielectric, which is an organic-ceramic laminate based on a woven glass reinforcement with a thickness of 0.76 mm, a copper thickness of 35 μ m, a dielectric constant of 3.5, and a dissipation factor of 0.0018.

All the circuits were performed with RF frequency of 2.6 GHz, LO frequency of 2.5 GHz, and IF frequency of 100 MHz, and the DC-block and DC-feed circuits had a chip capacitance of 100 pF and a chip inductance of 100 nH.

Figure 4.19 shows the conventional cascode FET mixer that was fabricated on printed substrate. The conventional cascode FET mixer that was fabricated under circuit conditions for the simulation had a well-known RF performance with high conversion gain, high linearity, a low noise figure, and poor LO-to-IF isolation. The fabricated conventional cascode FET mixer shown in Fig. 4.19, however, was designed as a circuit with high conversion gain and high linearity, for comparison of the cascode FET mixer using new circuit configuration.



Figure 4.19 The fabricated conventional cascode FET mixer on printed substrate.



Figure 4.20 The fabricated cascode FET mixer using new circuit configuration on printed substrate.

Figure 4.20 shows the cascode FET mixer using new circuit configuration that was fabricated on printed substrate. The cascode FET mixer using new circuit

configuration was also fabricated under circuit conditions for the simulation. It had an enhanced RF performance with higher conversion gain at lower LO power, lower noise figure, and higher LO-to-IF isolation, without LO rejection filter, as opposed to the conventional cascode FET mixer.



Figure 4.21 The comparison of the measured conversion gain characteristics of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer on printed substrate.

Figure 4.21 shows the comparison of the measured conversion gain characteristics of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. The measured conversion gain was a function of LO power, as shown in Fig. 4.21. The conventional cascode FET mixer showed a maximum conversion gain of 5.6 dB when the LO power was 1 dBm and the RF power was -40 dBm. The cascode FET mixer using new circuit configuration, on the other hand, showed a maximum conversion gain of 8.1 dB when the LO power was -1 dBm and the RF power was -40 dBm. The results showed a difference between the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer using new circuit configuration and the conventional cascode FET mixer using new circuit configuration and the conventional cascode FET mixer using new circuit configuration and the conventional cascode FET mixer, which had high maximum conversion gain of 2.5

dB.

In the results shown in Fig. 4.5 and 4.21, a difference was observed between the measured conventional cascode FET mixer, which had maximum conversion gain of 1.55 dB, low gain compared with the corresponding simulation result, and the cascode FET mixer using new circuit configuration. A difference was observed between the measured cascode FET mixer using new circuit configuration, which had maximum conversion gain of 3.64 dB, low conversion gain compared with the corresponding simulation result, conventional cascode FET mixer.

In these results, the low conversion gain characteristic is not considered accurate and is thus not considered indicative of the loss of the transmission line by the substrate, the loss of the connector between the port and the substrate, and the loss of soldering.



Figure 4.22 The comparison of the measured LO-to-IF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer on printed substrate.

Figure 4.22 shows the comparison of the measured LO-to-IF isolation characteristic of the cascode FET mixer using new circuit configuration and the

conventional cascode FET mixer. The measured LO-to-IF isolation characteristic was a function of LO power, as shown in Fig. 4.22. The conventional cascode FET mixer showed LO-to-IF isolation characteristic of -26.6 dBm when the maximum conversion gain was 5.6 dB at the LO power of 1 dBm and the RF power of -40 dBm. The cascode FET mixer using new circuit configuration, on the other hand, showed LO-to-IF isolation characteristic of -32.3 dBm when the maximum conversion gain was 8.1 dB at the LO power of -1 dBm and the RF power of -40 dBm.

These results show a difference between the cascode FET mixer using new circuit configuration, which had a high LO-to-IF isolation characteristic of 5.7 dB, and the conventional cascode FET mixer. The cascode FET mixer using new circuit configuration thus showed higher LO-to-IF isolation characteristic than the conventional cascode FET mixer.

The results shown in Fig. 4.6 and 4.22 show a difference between the measured conventional cascode FET mixer, which had LO-to-IF isolation characteristic of 19.04 dB, very high LO-to-IF isolation characteristic compared with the corresponding simulation result. Especially, for the measurement, the conventional cascode FET mixer was designed to have a $\lambda/4$ open stub with a quarter wavelength for LO rejection because of the influx of high LO signals, for the stable operation of the conventional cascode FET mixer. It thus showed high LO-to-IF isolation characteristic due to the LO rejection filter at the drain of FET₂.

A difference was observed between the measured cascode FET mixer using new circuit configuration, which had LO-to-IF isolation characteristic of 8.34 dB, lower than the corresponding simulation result, and the conventional cascode FET mixer.

Figure 4.23 shows the comparison of the measured LO-to-RF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer. The measured LO-to-RF isolation characteristic

was a function of LO power, as shown in Fig. 4.23.



Figure 4.23 The comparison of the measured LO-to-RF isolation characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer on printed substrate.

The conventional cascode FET mixer showed LO-to-RF isolation characteristic of -13.9 dBm when the maximum conversion gain was 5.6 dB at the LO power of 1 dBm and the RF power of -40 dBm. The cascode FET mixer using new circuit configuration, on the other hand, showed LO-to-RF isolation characteristic of -18.9 dBm when the maximum conversion gain was 8.1 dB at the LO power of -1 dBm and the RF power of -40 dBm.

These results show a difference between the proposed cascode FET mixer, which had high LO-to-RF isolation characteristic of 5 dB, and the conventional cascode FET mixer. The cascode FET mixer using new circuit configuration and the conventional cascode FET mixer both showed high LO-to-RF isolation characteristics.

In the results shown in Fig. 4.7 and 4.23, a difference was observed between the measured conventional cascode FET mixer, which had LO-to-RF isolation

characteristic of 3.89 dB, lower than the corresponding simulation result, and the proposed cascode FET mixer using new circuit configuration, which had LO-to-RF isolation characteristic of 6.5 dB, lower than the corresponding simulation result.



Figure 4.24 The comparison of the measured P_{1dB} characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer on printed substrate.

Figure 4.23 shows the comparison of the measured P_{1dB} characteristic of the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer, fabricated on printed substrate. The measured P_{1dB} characteristic was a function of RF power, as shown in Fig. 4.23. The conventional cascode FET mixer showed P_{1dB} characteristic where the input RF and output IF power were -11 and -4.7 dBm, respectively. This was the operation condition when the conversion gain was 3.1 dB at the LO power of -2 dBm and the RF power of -40 dBm. The cascode FET mixer using new circuit configuration, on the other hand, showed P_{1dB} characteristic where the input RF and output IF power were -17.4 dBm, respectively. This was the operation condition when the conversion gain was 3.2 dB at the LO power of -8 dBm and the RF power of -40 dBm.

The results shown in Fig. 4.9, 4.10, and 4.23 show a difference between the conventional cascode FET mixer, which had output IF power of 0.63 dB, similar to the corresponding simulation result under the same conditions, and the cascade FET mixer using new circuit configuration. A difference was observed between the two mixers, with the cascode FET mixer using new circuit configuration showing lower output IF power of 2.08 dB compared with the corresponding simulation result, under the same conditions.

Table 4.2 The summary of measured RF performances for the cascode FET mixer using new circuit configuration and the conventional cascode FET mixer.

	The proposed	The conventional
Characteristic	cascode FET mixer	cascode FET mixer
DC power consumption [mW]	9.5	9.4
Max. conversion gain [dB]	8.1	5.6
	(at LO power = -1)	(at LO power= +1)
LO-to-IF isolation [dBm]	-32.3	-26.6
	(at LO power = -1)	(at LO power = $+1$)
LO-to-RF isolation [dBm]	-18.9	-13.9
	(at LO power = -1)	(at LO power = $+1$)
P _{1dB} [dBm]	-17.4	-4.7
	(at RF power = -22)	(at RF power = -11)
	(at LO power = -1)	(at LO power = $+1$)

Table 4.2 is the summary of the measured RF performances for the cascode FET mixer using new circuit configuration and for the conventional cascode FET mixer, which are exhibited for comparison purposes.

Chapter 5.

Conclusion



This study was conducted for the purpose of developing a circuit for the wireless communication system with enhanced RF performance due to the use of the cascode FET mixer using new circuit configuration.

The cascode FET mixer using new common-source and -drain circuit configuration is shown herein. The results of the design and measurement are also exhibited to verify the RF performances. The simulation results showed that the cascode FET mixer using new circuit configuration had enhanced RF performances compared with the conventional cascode FET mixer. The proposed new circuit configuration consisting of common-source and -drain is reported in this thesis for the first time.

The cascode FET mixer using new common-source and -drain circuit configuration is an indispensable circuit for the wireless communication system, which requires low power consumption due to the high RF performance with low power LO signal, as opposed to the conventional cascode FET mixer. It showed higher conversion gain with lower LO power than the conventional cascode FET mixer. Further, it does not need a local oscillator with large output power as it needs lower input LO power than the conventional cascode FET mixer. Thus, it is an important component of wireless communication system, which requires effective power consumption.

The cascode FET mixer using new circuit configuration also showed very low noise figure than the conventional cascode FET mixer. It uses only a FET, which produces the effect to have very low noise figure due to the thermal and shot noise by an active device. The cascode FET mixer using new circuit configuration also showed very high LO-to-IF isolation without a LO rejection filter compared with the conventional one. It showed good LO-to-RF isolation. The cascode FET mixer

using new circuit configuration showed low output IF power and low linearity for the output IF power of the fundamental and third-order intermodulation frequencies, low than those of the conventional one. It also showed the low output IF power spectrum for the intermodulation distortion of the low- and up-side bands, as opposed to the conventional one. It showed that each reflection coefficients were about -30 dB for the RF frequency of 2.6 GHz, the LO frequency of 2.5 GHz, and the IF frequency of 100 MHz.

The study results show that the new cascode FET mixer with enhanced RF performance using new common-source and -drain circuit configuration can achieve high performance without an addition to any other circuit. Further, the cascode FET mixer using new circuit configuration has various advantages and enhanced performance aspects, as opposed to the conventional mixer, and shows enhanced RF performance under the same conditions, for circuit design. Especially, the cascode FET mixer using new circuit configuration shewed an indispensable circuit for a wireless communication system, which requires low power consumption due to the high RF performance by lower LO signal power. Therefore, the cascode FET mixer using new common-source and -drain circuit configuration showed enhanced and effective performance and is certainly needed to improve the efficiency of the wireless communication system, which has low efficiency due to its mobility and limited power.

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